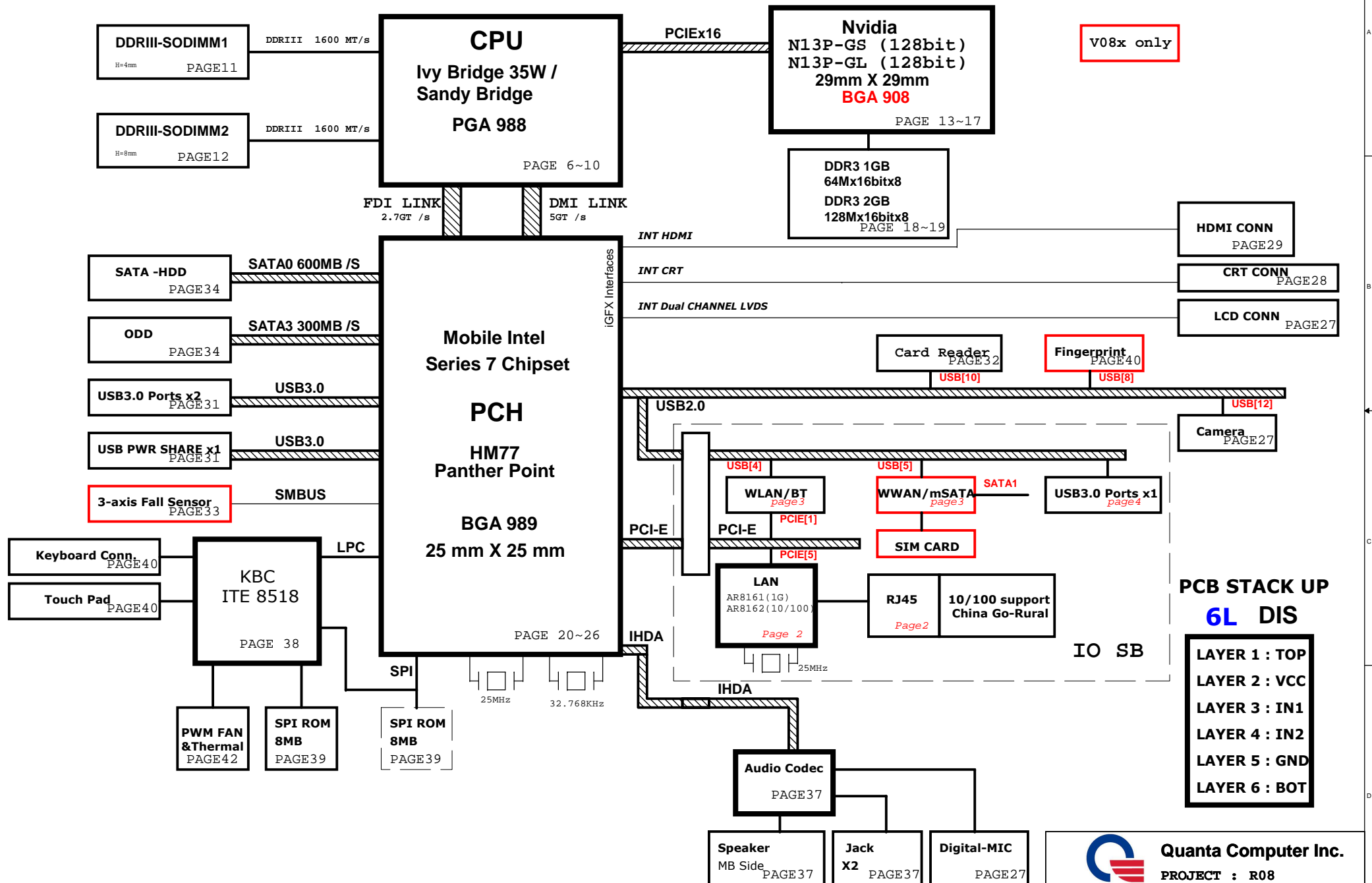
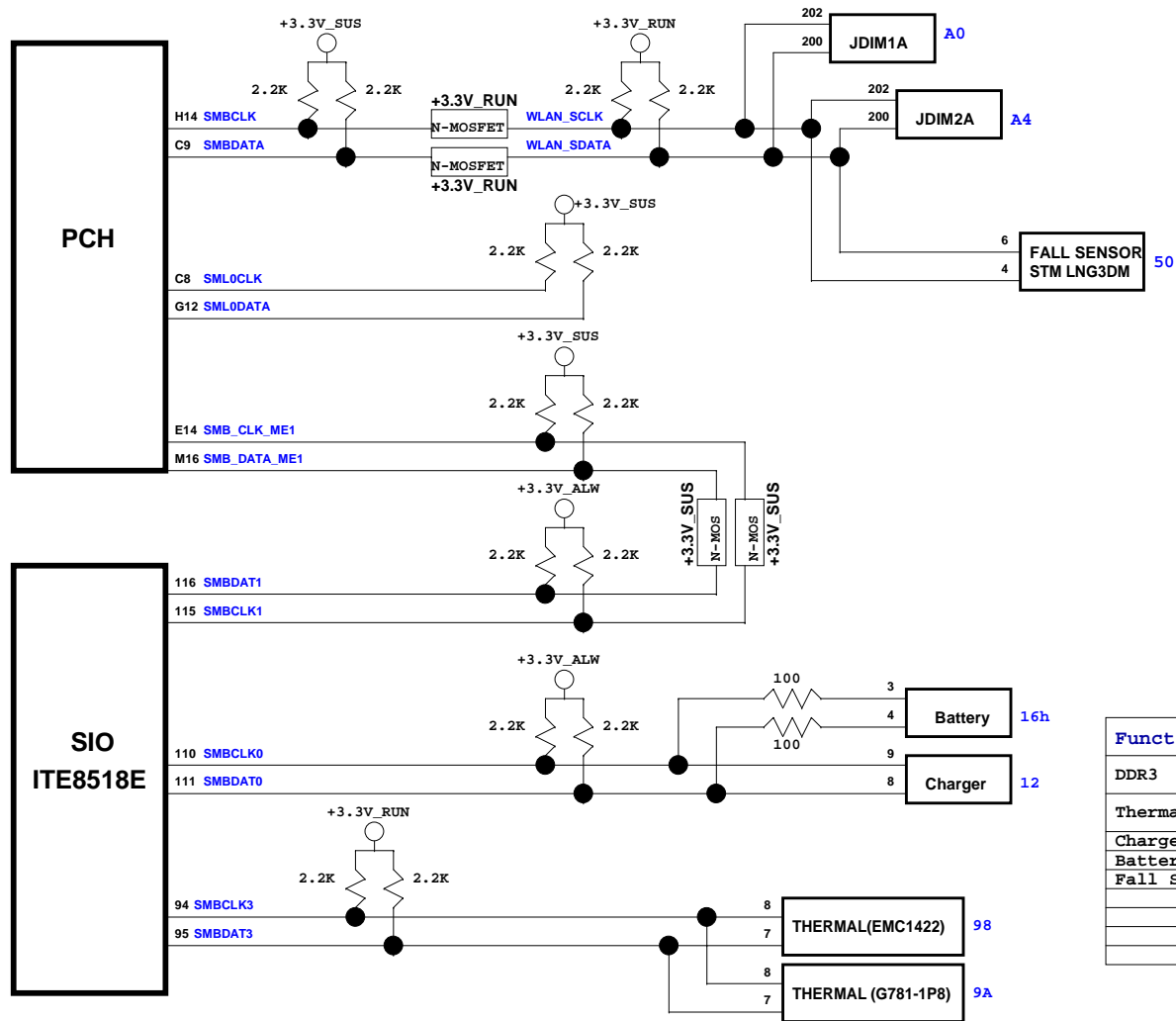


R08/V08 BLOCK DIAGRAM

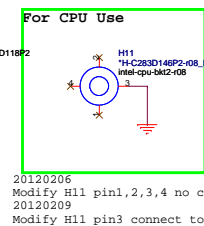
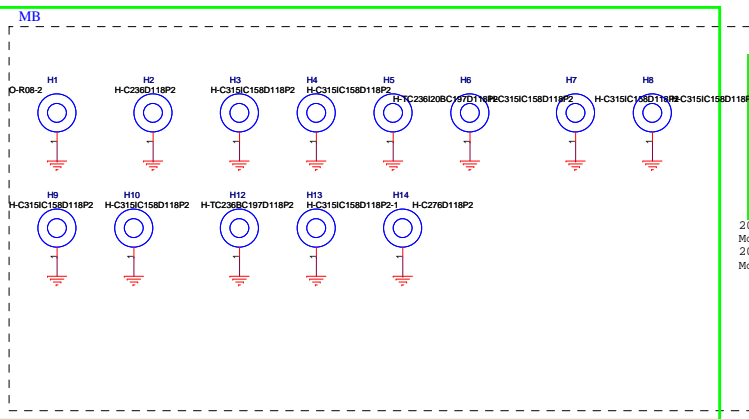
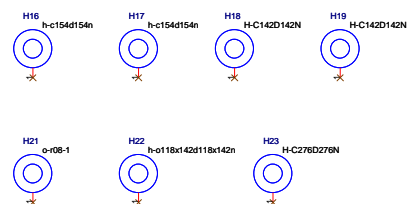


Quanta Computer Inc.
PROJECT : R08

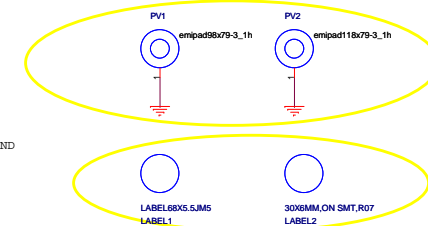


Function	IC	SMBus Address
DDR3	JDIM1A JDIM2A	A0h A4h
Thermal IC	EMC1422 G781-1P8	1001100xb (98h) 1001101xb (9Ah)
Charge IC	BQ24707ARGRR	0b0001001x (0x12h)
Battery	Battery	16h
Fall Sensor	STM LNG3DM	01010000 (50h)

SCREW PAD



20120204
Modify PV1 PV2 subsystem ID to OTH

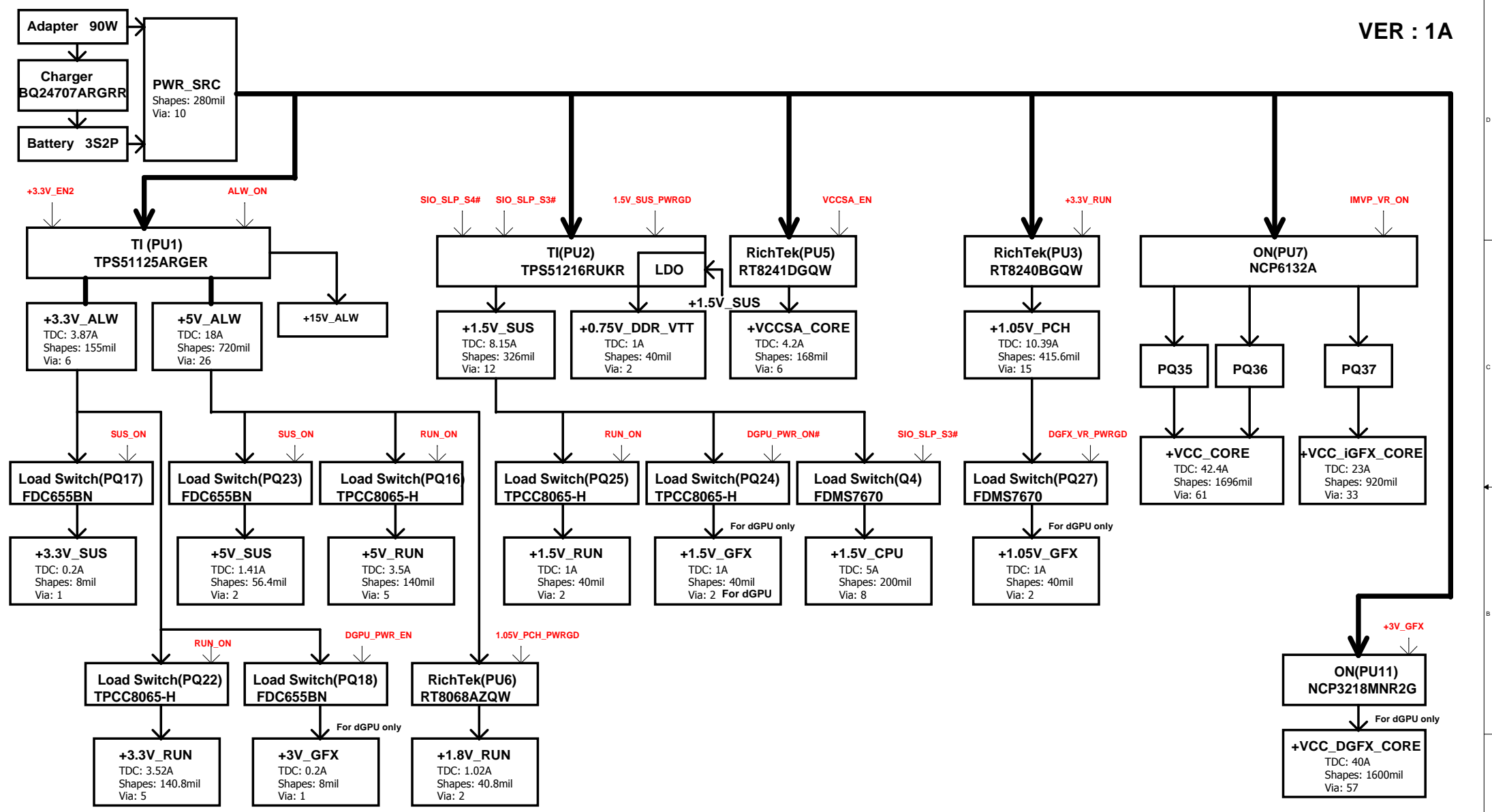


20120204
Add two label PV HCR07003010 and RCM5004013

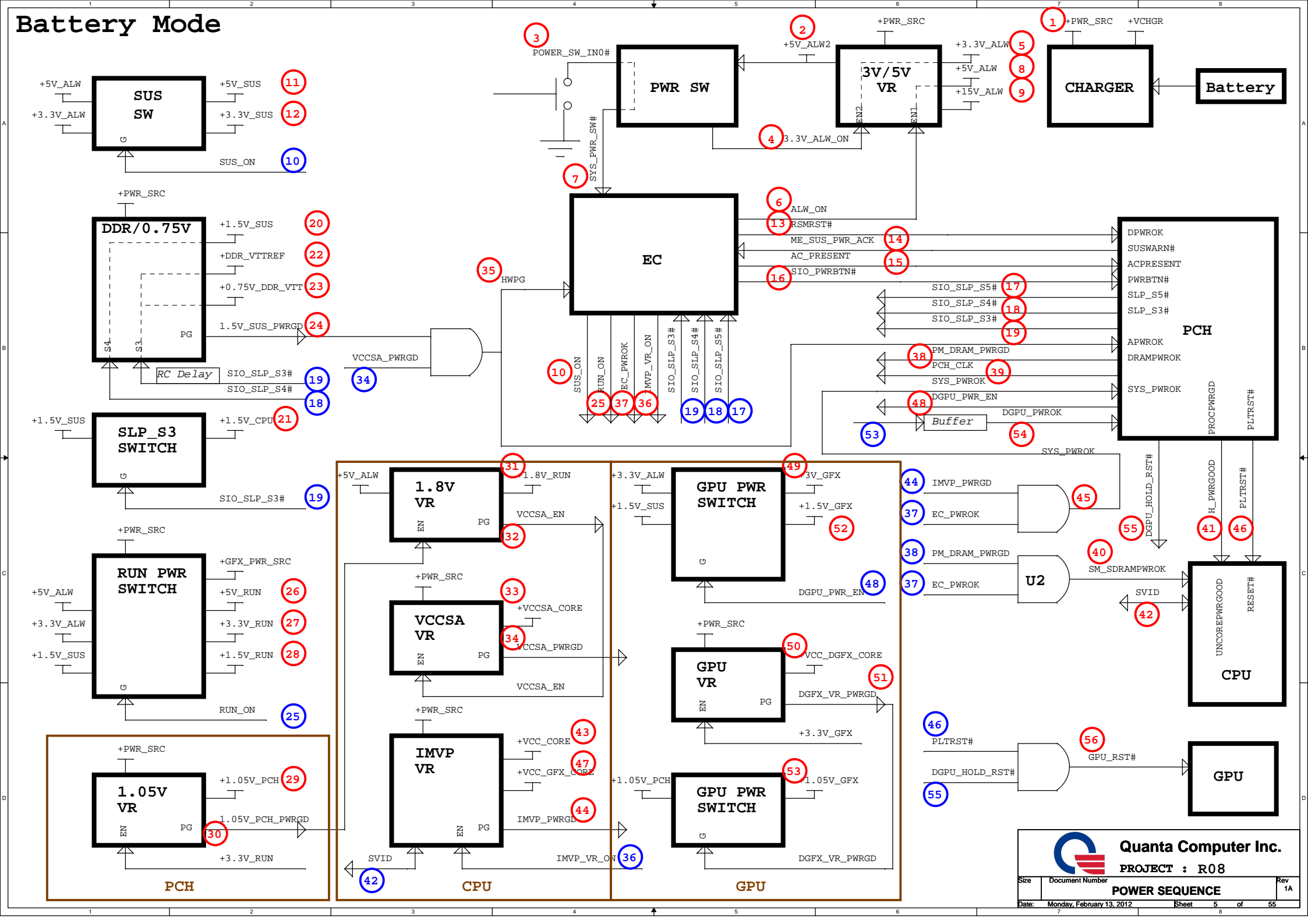
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0/eSATA/ Power share/ debug port)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT)
USB5	MiniCard 2 (WWAN/WiMAX)
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	Touch panel (NC, for debug)
USB10	Card Reader
USB11	Express Card (NC)
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD
SATA4	eSATA (NC)
SATA5	NC

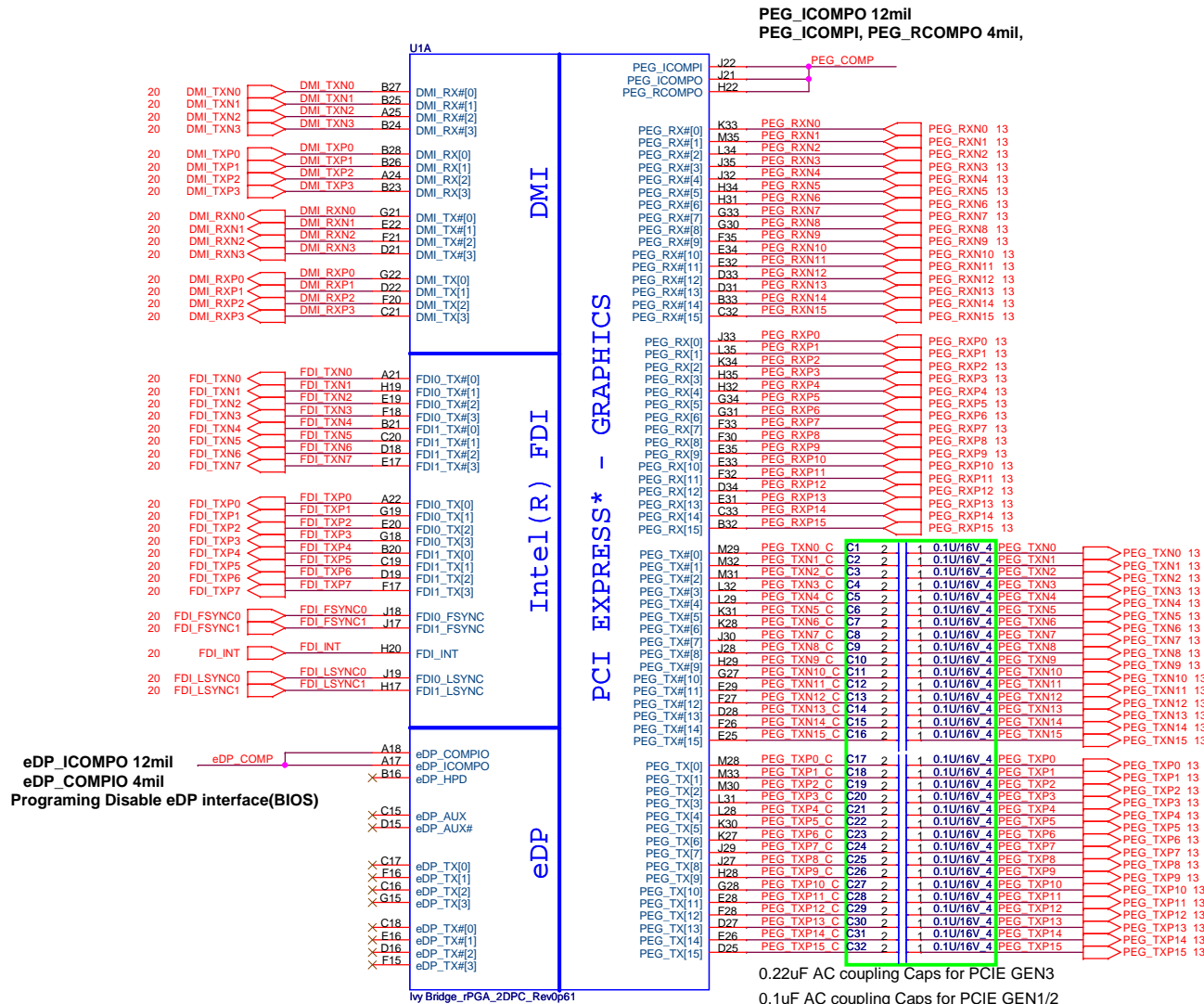
PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	WWAN (NC)
PCIE 3	Card reader (NC)
PCIE 4	NC
PCIE 5	LAN
PCIE 6	Express card (NC)
PCIE 7	NC
PCIE 8	NC



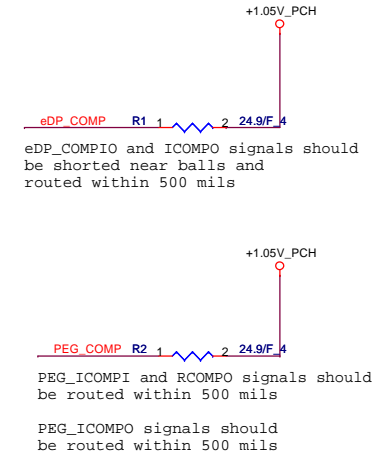
Battery Mode



Ivy Bridge Processor (RESERVED, CFG)



DP & PEG Compensation



eDP Hot-plug (Disable)

CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

VGA (U3)	AC coupling Cap	PN	TX location	RX location(page13)
N13P-GL	0.1uF	CH4103K1B08	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185
N13P-GS	0.22uF	CH4223K1B00	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185

Ivy Bridge Processor (CLK,MISC,JTAG)

SNB_IVB# N.A at SNB EDS #27637 0.7v1

23 H_SNB_IVB# ← H_SNB_IVB# C26
38 H_CPUDET# ← H_CPUDET# AN34

TP1 CATERR# ← CATERR# AL33

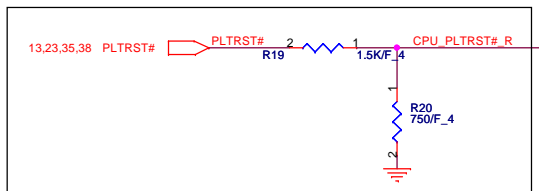
38 PECI_EC ← PECI_EC R6 1 2 43 4 PECI_EC_R AN33

38,52,54 IMVP7_PROCHOT# ← IMVP7_PROCHOT# R7 1 2 56 4 H_PROCHOT# AL32

Over 130 degree C will drive low
25 PM_THRMTRIP# ← PM_THRMTRIP# AN32

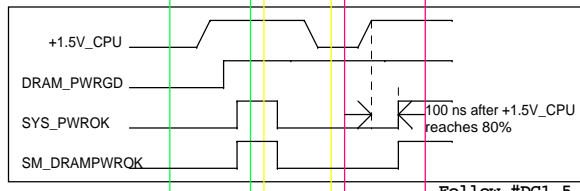
20 H_PM_SYNC ← H_PM_SYNC AM34

25 H_PWRGOOD ← H_PWRGOOD AP33
10K 4 2 1 R17
SM_DRAMPWROK V8



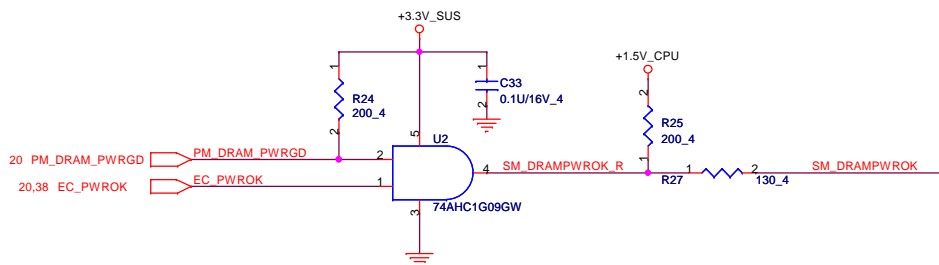
Intel spec VinH min = VCCIO X 0.7

C854 2 1 *100P/50V 4 NC H_PROCHOT#
C860 2 1 *100P/50V 4 NC CPU_PLTRST# R



Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P128
DDR Power Gating Topology



MISC

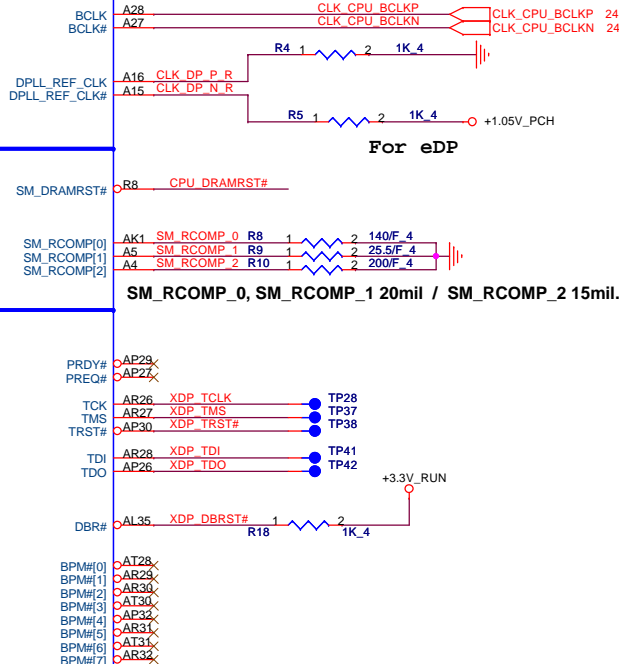
THERMAL

PWR MANAGEMENT

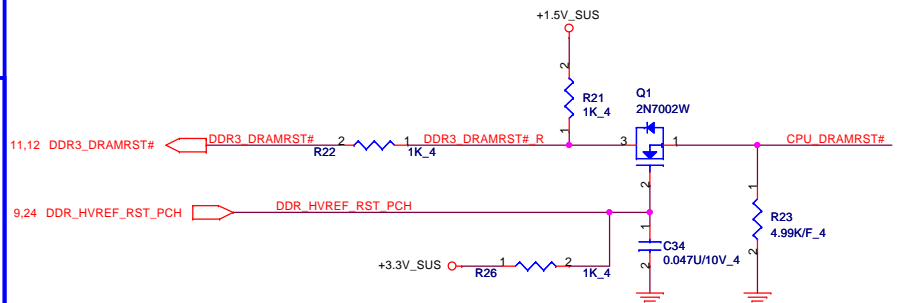
CLOCKS

DDR3 MISC

JTAG & BPM

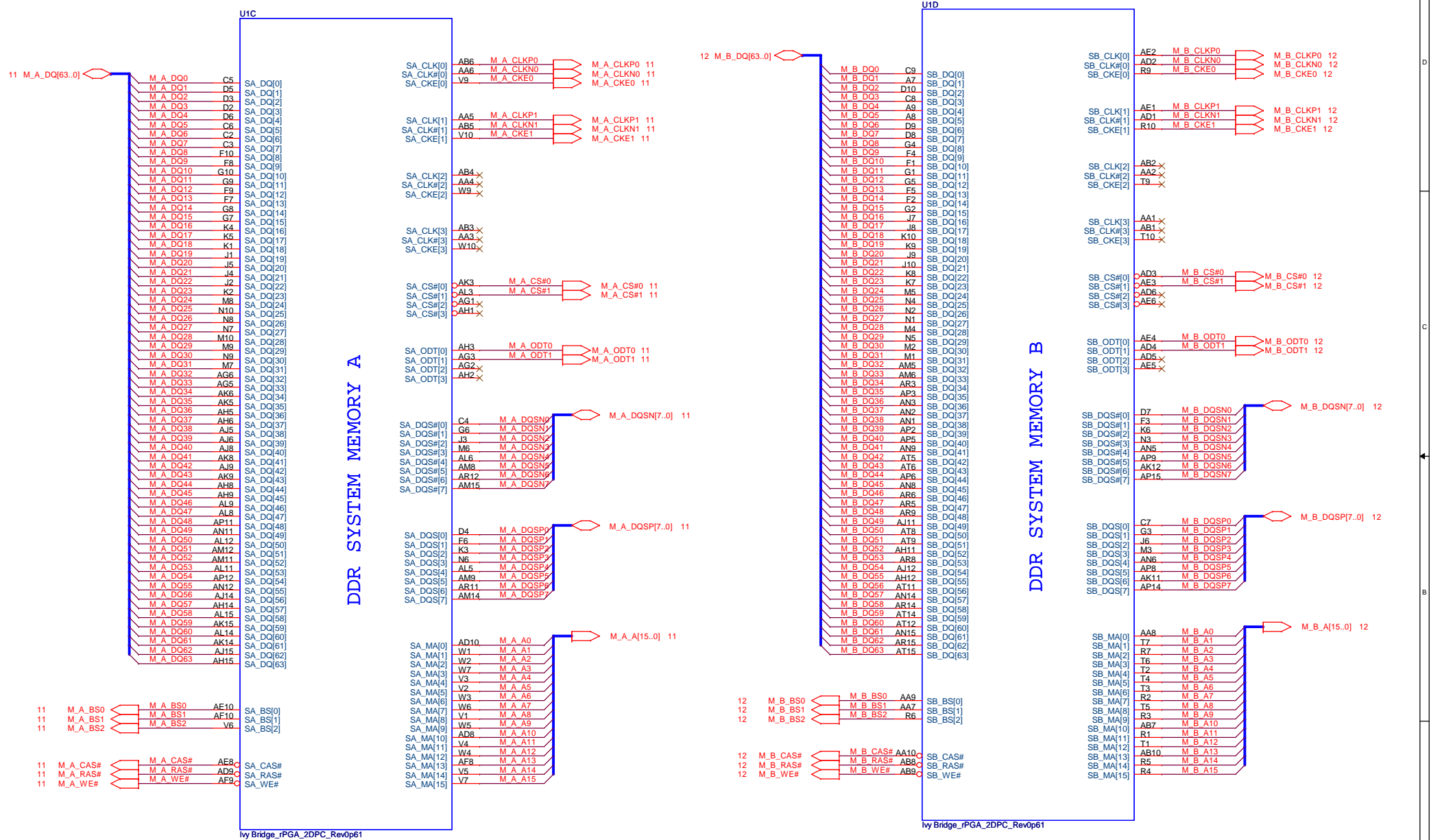


Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration



Quanta Computer Inc.
PROJECT : R08

Ivy Bridge Processor (DDR3)



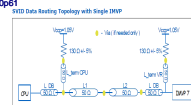
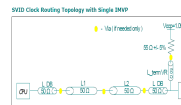
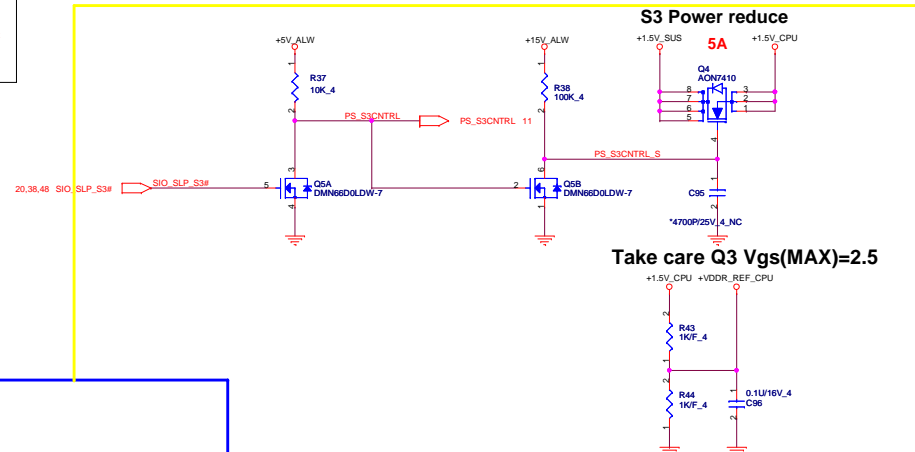
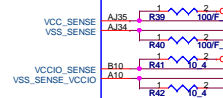
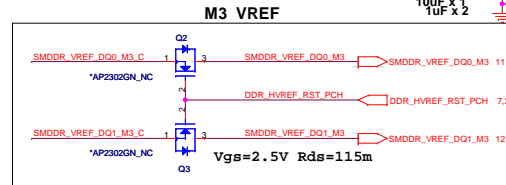
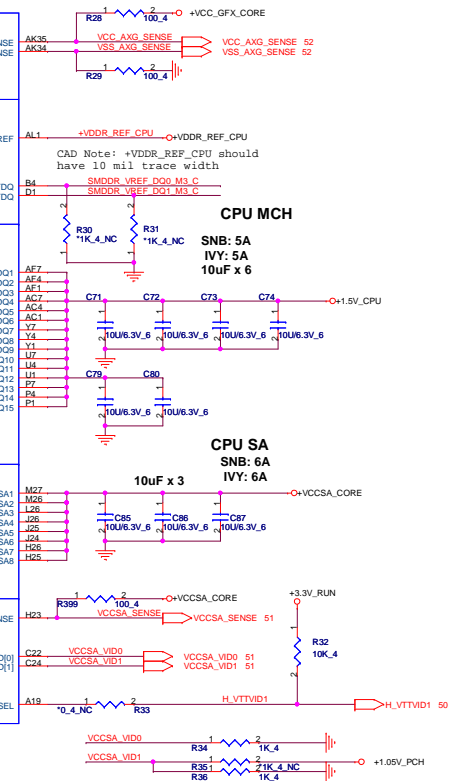
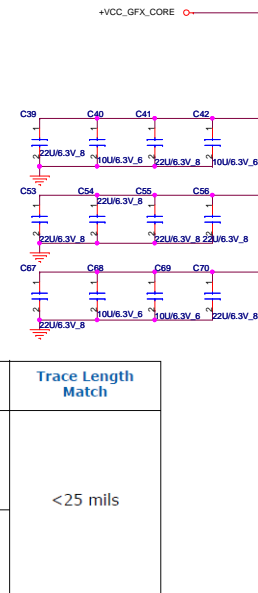
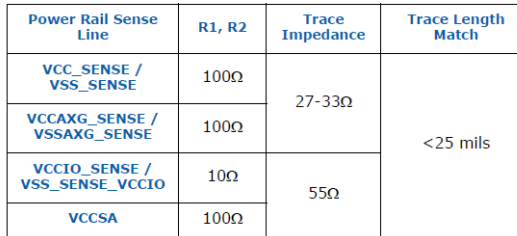
Quanta Computer Inc.
PROJECT : R08

Ivy Bridge Processor (GRAPHIC POWER)

1.05V_PCH
SNB: 8.5A
IVY: 8.5A
10F x12

CPU VGT
SNB: 21.5A
IVY: 33A
10uF x 12

POWER



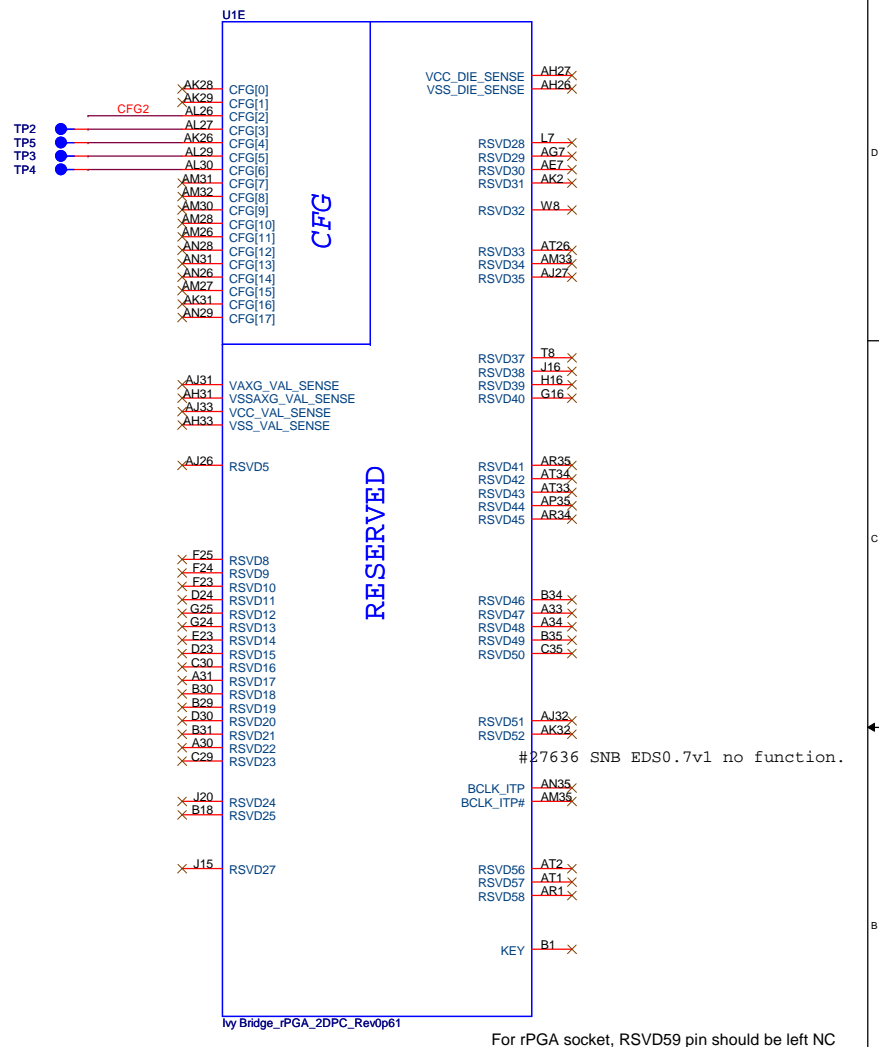
SVID CLK

SVID DATA

SVID ALERT

Take care Q3 $V_{gs}(\text{MAX})=2.5$

Ivy Bridge Processor (RESERVED, CFG)



```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

The CFG signals have a default value of '1' if not terminated on the board.



PROJECT : R08

Rev
1A

Date: Monday, February 13, 2012 Sheet 10 of 55

H=8mm,RVS

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

8 M_A_BS0
8 M_A_BS1
8 M_A_BS2
8 M_A_CS#0
8 M_A_CS#1
8 M_A_CLKP0
8 M_A_CLKP1
8 M_A_CLKN1
8 M_A_CKE0
8 M_A_CKE1
8 M_A_CAS#
8 M_A_RAS#
8 M_A_WE#

8 M_A_ODT0
8 M_A_ODT1

8 M_A_DQSP[7..0]

8 M_A_DQSN[7..0]

JDIM1A

A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC#
A13
A14
A15

BA0
BA1
BA2
S0#
S1#
CK0
CK0#
CK1
CK1#
CKE0
CKE1
CAS#
RAS#
WE#

DIMM0_SA0
DIMM0_SA1
SCL
SDA

M_A_ODT0
M_A_ODT1

DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7

DQS0
DQS1
DQS2
DQS3
DQS4
DQS5
DQS6
DQS7

DQS#0
DQS#1
DQS#2
DQS#3
DQS#4
DQS#5
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DQS#7

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DQS#4
DQS#5
DQS#6
DQS#7

PC2100 DDR3 SDRAM SO-DIMM
(204P)

DDR3-DIMM0

12

M_A_DQ[63..0] 8

M3 VREF

M1 VREF

S3 Power reduce

+0.75V_DDR_VTT

R50
22_4

Q7

PS_S3CNTRL

2N7002W

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

PS_S3CNTRL 9

+1.5V_SUS

JDIM1B

VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDD10
VDD11
VDD12
VDD13
VDD14
VDD15
VDD16
VDD17
VDD18

VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34

VDDSPD
NC1
NC2
NCTEST

EVENT#
RESET#

VREF_DQ
VREF_CA

VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15

VTT1
VTT2

GND
GND

DDR3-DIMM0

203
204

+0.75V_DDR_VTT

205
206

GND
GND

207
208

GND
GND

209
210

GND
GND

211
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225
226

GND
GND

227
228

GND
GND

PC2100 DDR3 SDRAM SO-DIMM
(204P)

DDR3-DIMM0

203
204

+0.75V_DDR_VTT

205
206

GND
GND

207
208

GND
GND

209
210

GND
GND

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227
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229
230

GND
GND

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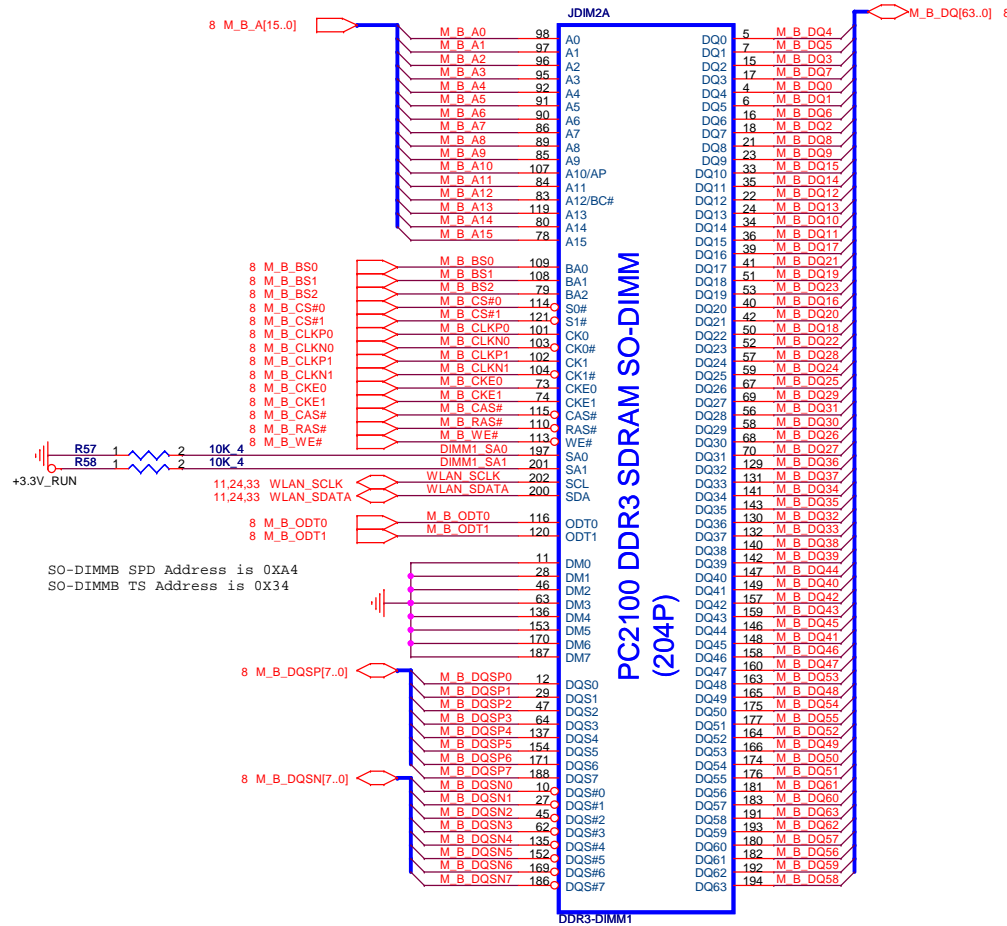
PROJECT : R08

Size Document Number Rev 1A

DDR3 DIMM-0

Date: Monday, February 13, 2012 Sheet 11 of 55

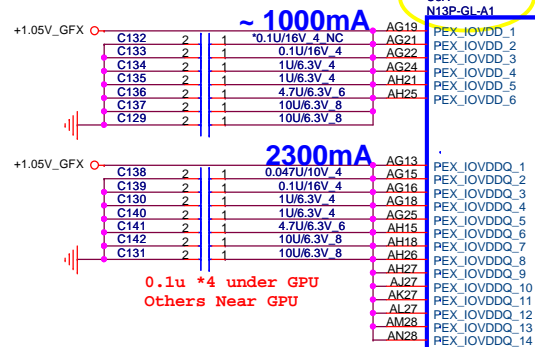
H=4mm,RVS



20120203
Change U3 to AJ0N13P0T02(N13P-GL)
20120204
Change U3 to AJ0N13P0T49(WINCON)

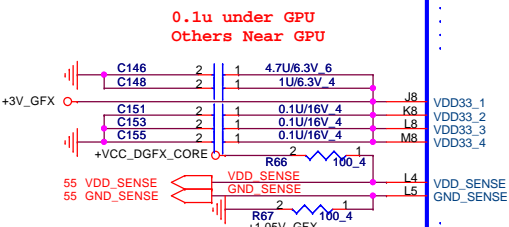
PEX_IOVDD+PEX_IOVDDQ >3.3A

U3A
N13P-GLA1

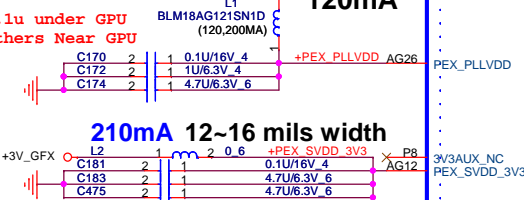


GB4-128

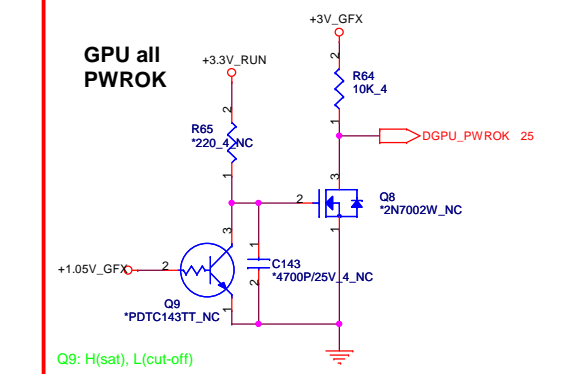
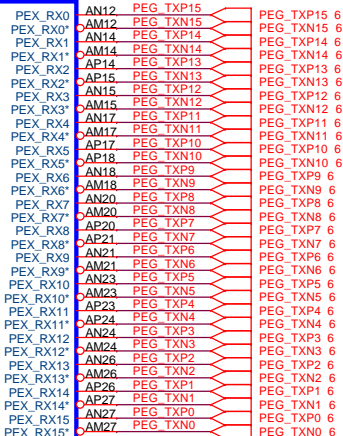
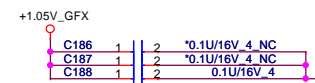
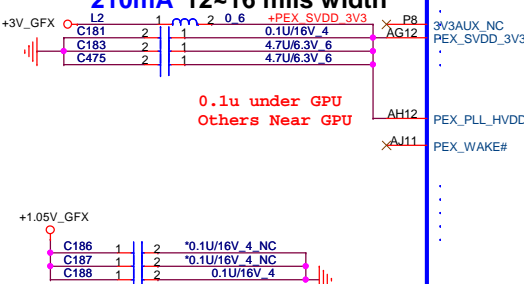
PCI EXPRESS



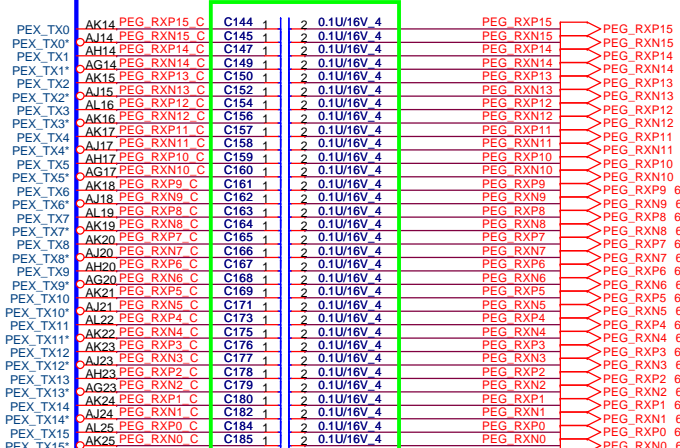
12~16 mils width
120mA



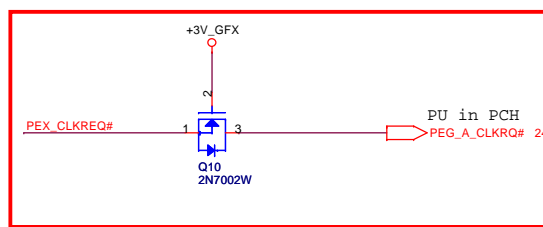
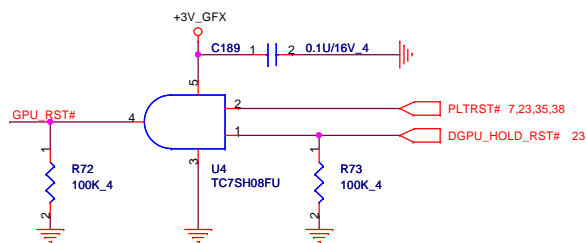
210mA 12~16 mils width



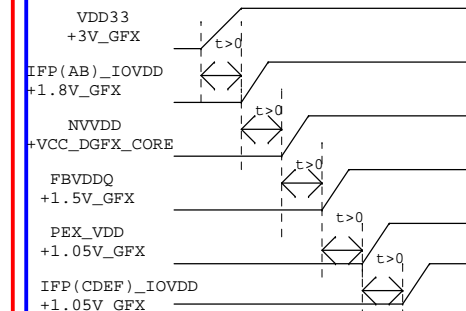
0.22uF AC coupling Caps for PCIE GEN3
0.1uF AC coupling Caps for PCIE GEN1/2



20120203
Change C144 C145 C147 C149 C150
C152 C154 C156 C157 C158
C159 C160 C161 C162 C163
C164 C165 C166 C167 C168
C169 C171 C173 C175 C176
C177 C178 C179 C180 C182
C184 C185 to 0.1U/16V_4(CH4103K1B08)

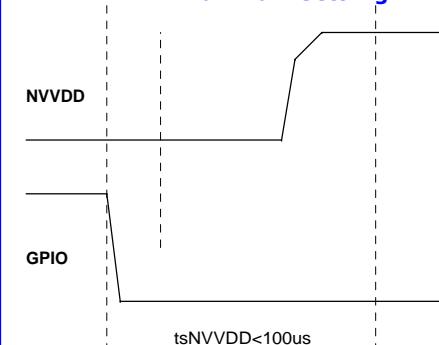


Power up sequence

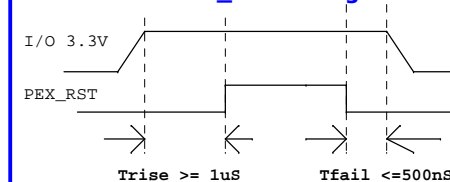


NB9M: VGACORE +0.90V (Normal) , +1.09V

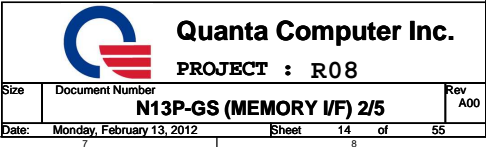
NVVDD Maximum Settling Time



PEX_RST timing



Quanta Computer Inc.
PROJECT : R08

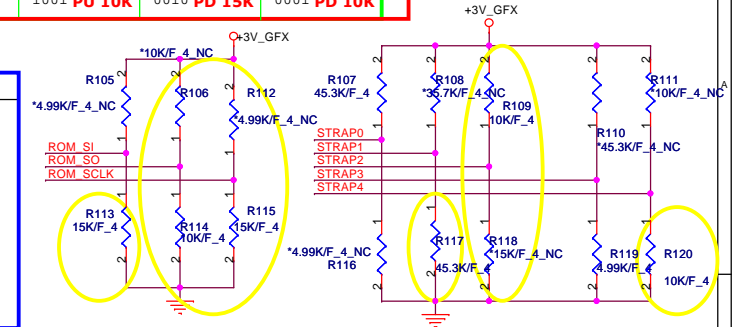


N13P-GL (AJ0N13P0T02)
N13P-GS for Turbo (AJ001070T00)

Strap Bit	Description
USER[3:0]	1111 EDID is used
3GIO_PADCFG [3:0]	0110 Notebook Default
PCI_DEVID[5:0]	D2 PCI Device ID
SORx_EXPOSED [3:0]	0000 Audio capability on each display port Not in use
DP_PLL_VDD33V	1 Default
PCIE_MAX_SPEED GEN3	1 PCIE Gen2/3 capable
PCIE_SPEED_CHANGE GEN3	0 Default
RAMCFG[3:0]	0010 Default Hynix1G
PCIE_PLL_TERMINATION	0 PCIE PLL termination disable (Default)
PEX_PLL_EN_TERM	0 No video BIOS ROM
SUB_VENDOR	0 No video BIOS ROM
FB[1:0]	01 Frame Buffer size Reserve
SMB_ALT_ADDR	0 Default (1GPU)
VGA_DEVICE	1 Default (non 3D)

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

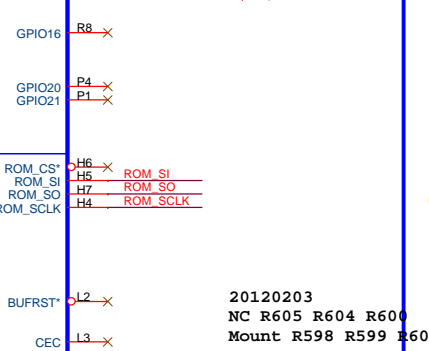
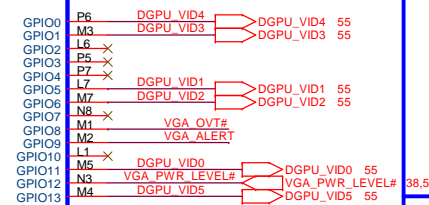
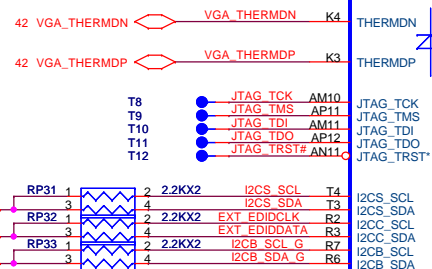


10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1% (0402)]
24.9K/F 4: CS32492FB16 [RES CHIP 24.9K 1/16W +1% (0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

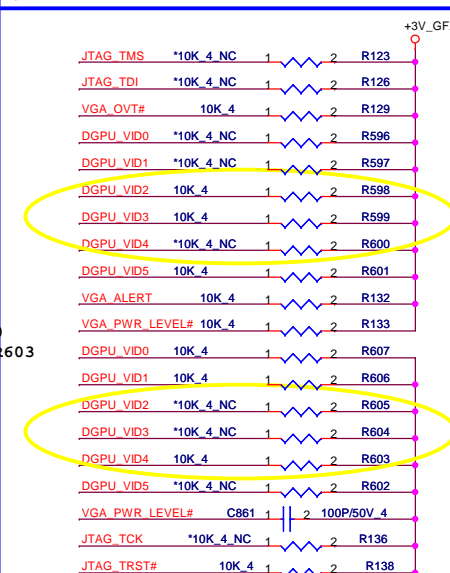
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1001
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0111
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Default: Hynix VRAM 2G (0110) VRAM Configuration Table


RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0000	Reserve	Reserved	Reserve	Reserve	PD 5K
0001	Reserve	Reserved	Reserve	Reserve	PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	AKD5LZWTW07	H5T1G63DFR-11C	PD 15K
0011	DDR3 64Mx16, 900MHz (G-die)	Samsung	AKD5EGGT509	K4W1G1646G-BC11	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	AKD5MGWTW06	H5T1Q638FR-11C	PD 35K
0111	DDR3 128Mx16, 900MHz	Samsung	AKD5MGWT507	K4W2G1646C-HC11	PD 45K



	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GL	0.95V	0	0	1	1	0	1
N13P-GS	0.9V	0	0	0	0	1	1



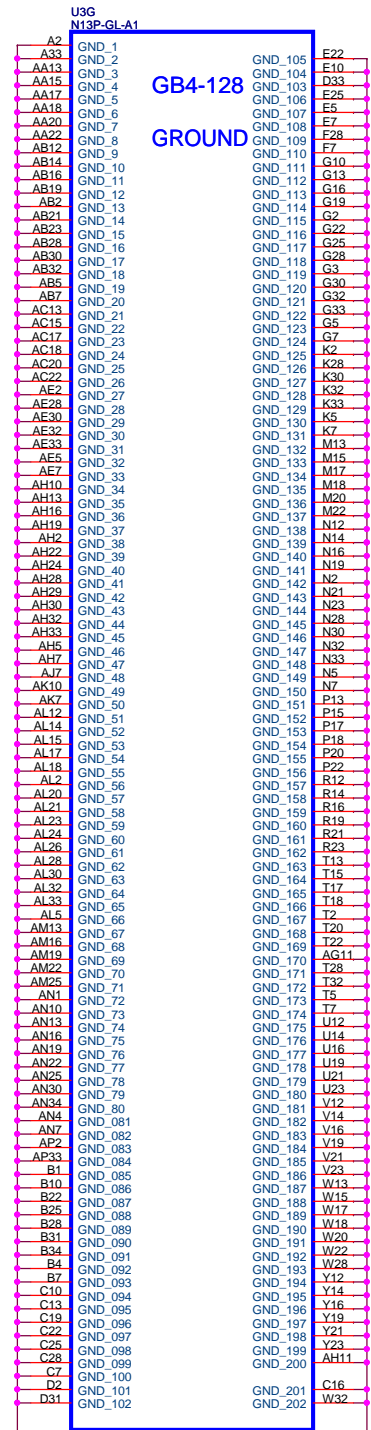
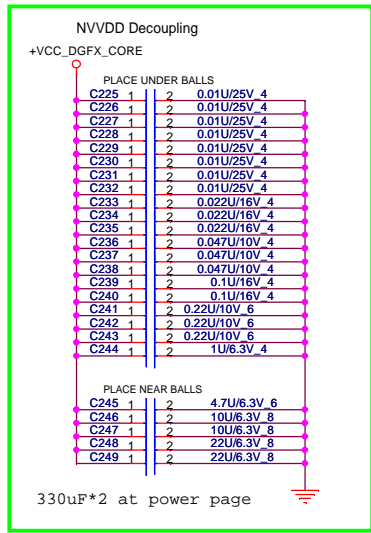
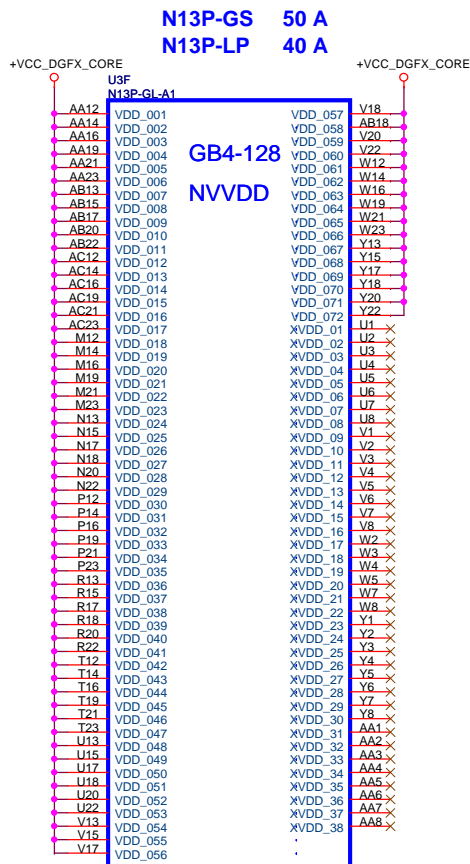
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	NVDD_VID4
1	IN	N/A	NVDD_VID3
2	OUT	HIGH	NC
3	OUT	HIGH	NC
4	OUT	HIGH	NC
5	OUT	N/A	NVDD_VID1
6	OUT	N/A	NVDD_VID2
7	OUT	N/A	NC
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	NC
11	OUT	N/A	NVDD_VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVDD_VID5

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PROJECT : R08

Size: Document Number: **N13P-GS (GPIO&STRAPS) 4/5** Rev: A00

Date: Monday, February 13, 2012 Sheet: 16 of 55

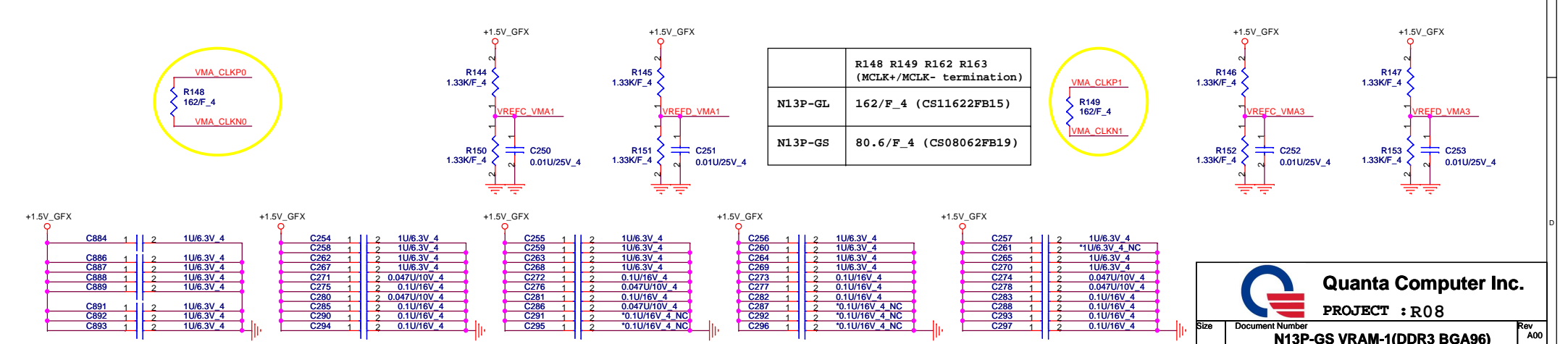
Check VID PU/PD



Change U6~U13 to AKD5LZWTW07 (hynix 1G)

```
14 VMA_DQ[63..0]  •
14 VMA_DM[7..0]   •
14 VMA_WDQS[7..0] •
14 VMA_RDQS[7..0] •
```

CHANNEL A: 512MB/1024MB DDR3



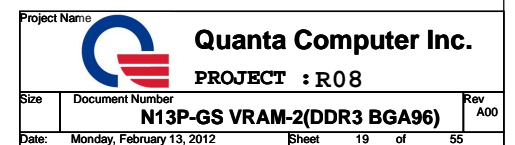
	R148 R149 R162 R163 (MCLK+/MCLK- termination)
N13P-GL	162/F_4 (CS11622FB15)
N13P-GS	80.6/F_4 (CS08062FB19)

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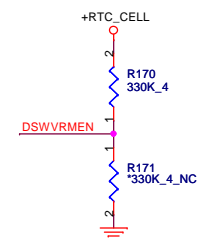
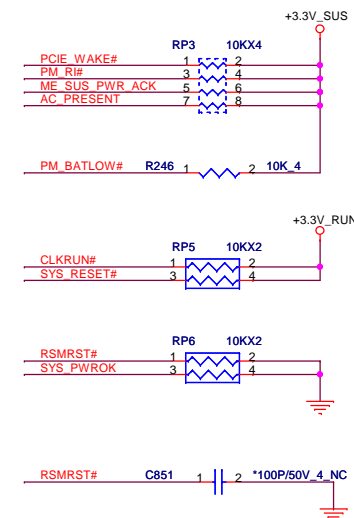
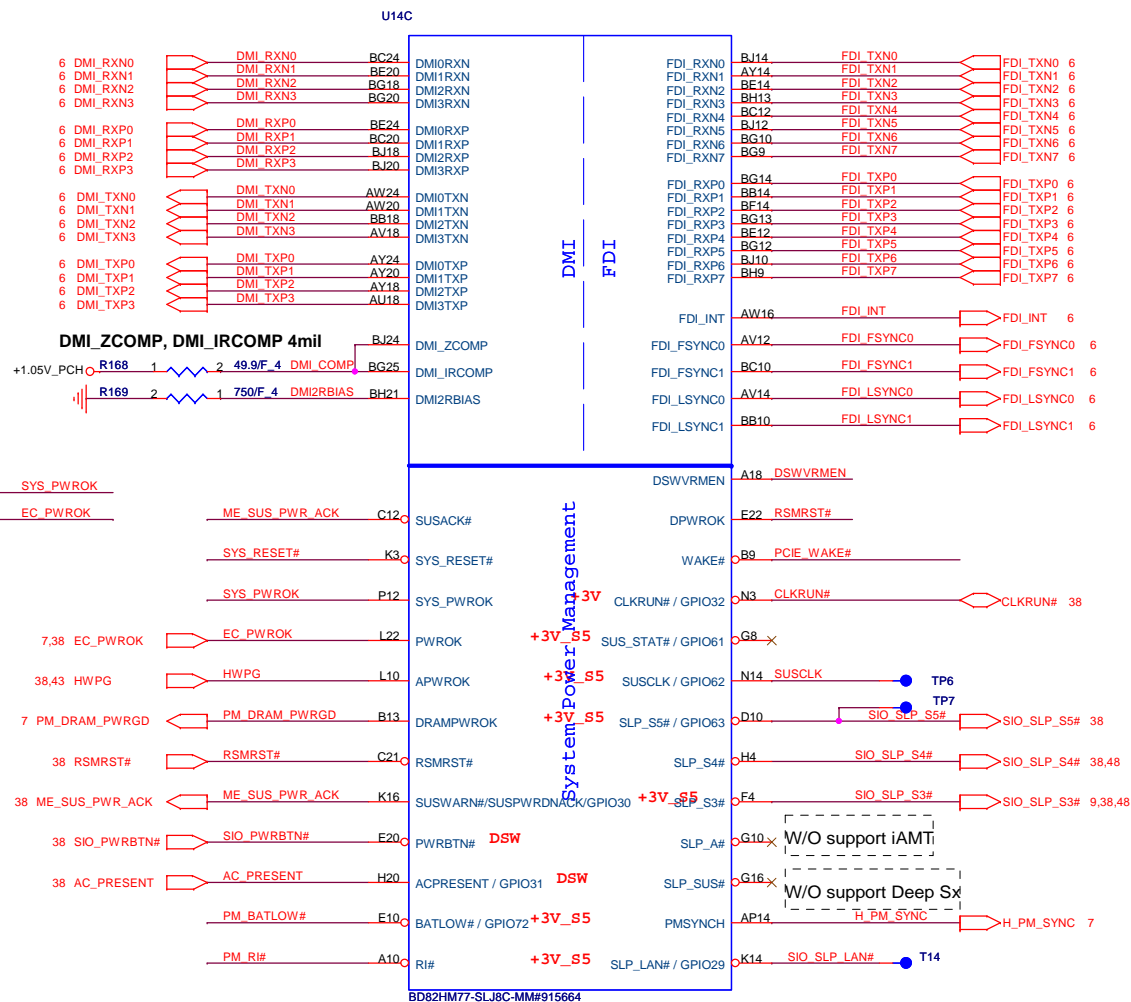
PROJECT : R08

Size	Document Number	Rev
	N13P-GS VRAM-1(DDR3 BGA96)	A00

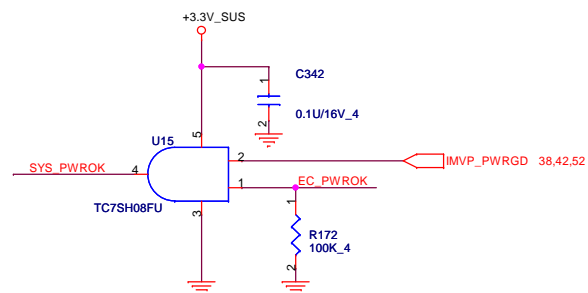
14 VMC_DQ[63..0]
14 VMC_DM[7..0]
14 VMC_WDQS[7..0]
14 VMC_RDQS[7..0]



Cougar Point/Panther Point (DMI,FDI,PM)



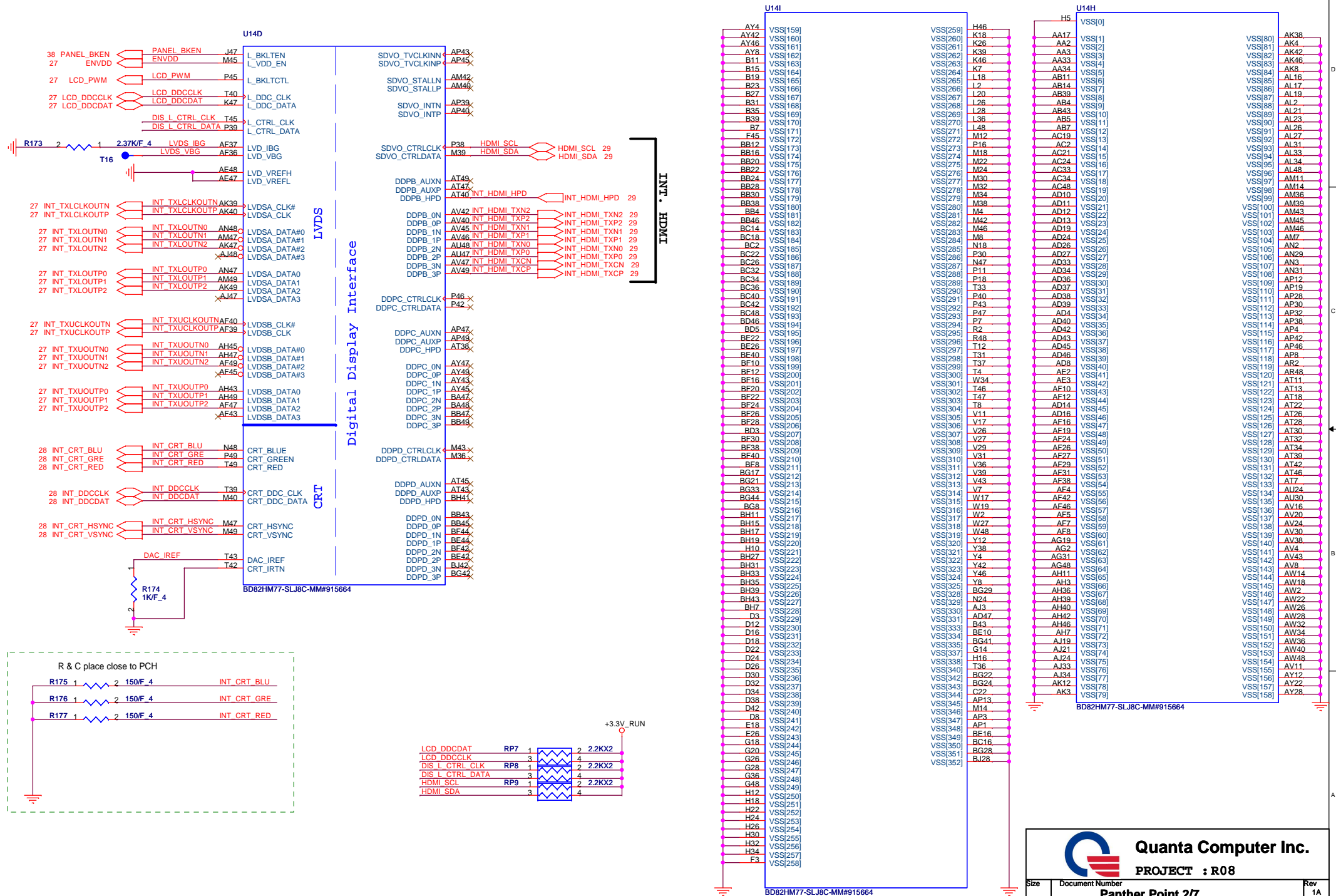
On Die DSW VR Enable
High = Enable (Default)
Low = Disable



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PROJECT : R08

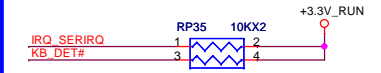
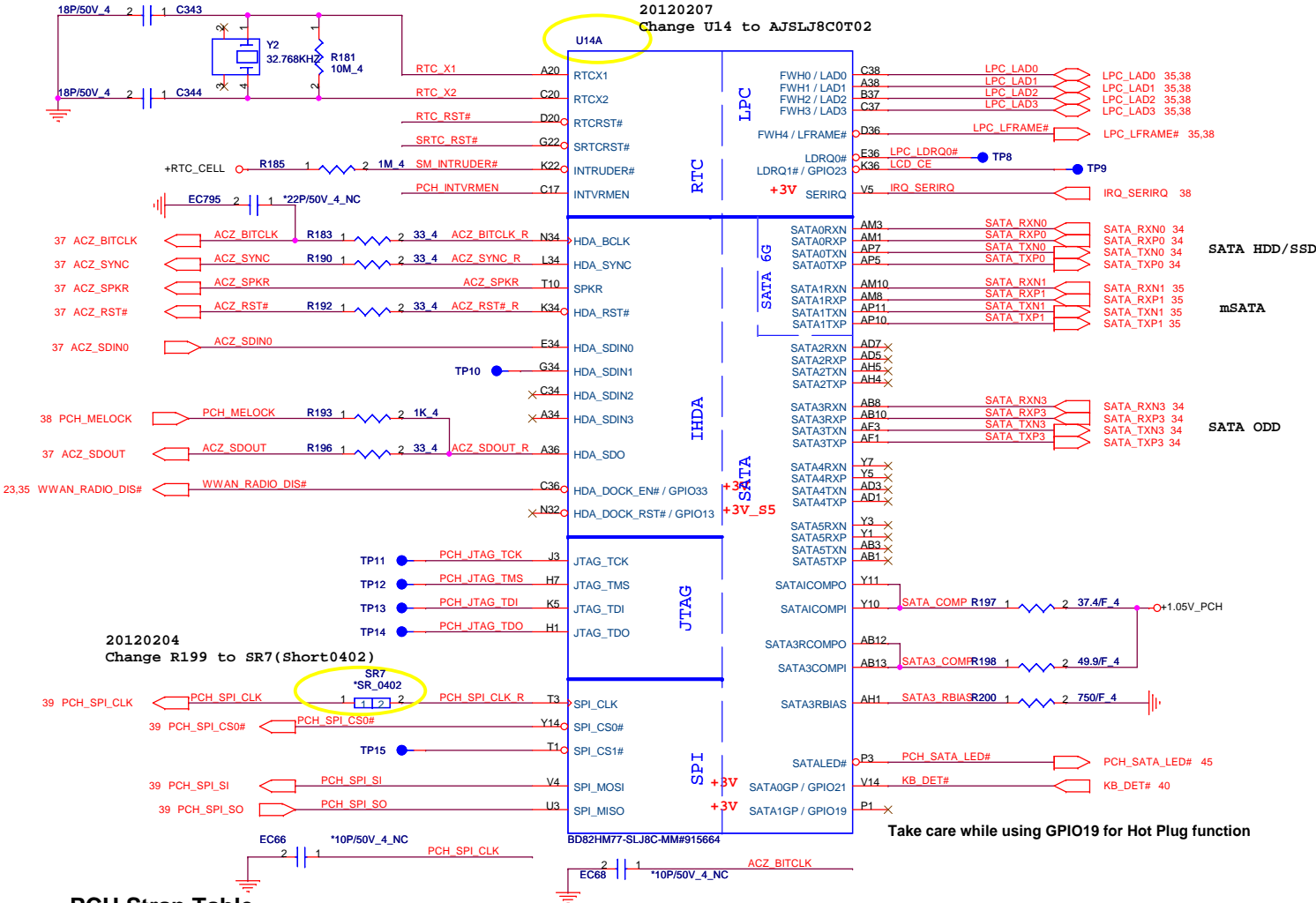
Size	Document Number Panther Point 1/7	Rev 1A
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Cougar Point/Panther Point (GND)

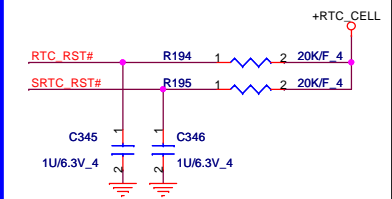


Cougar Point/Panther Point (HDA,JTAG,SATA)

20120204
Change U14 to AJ0QPEG0T07(WINCON)
20120207
Change U14 to AJSLJ8C0T02



MP remove(Intel)(JTAG)

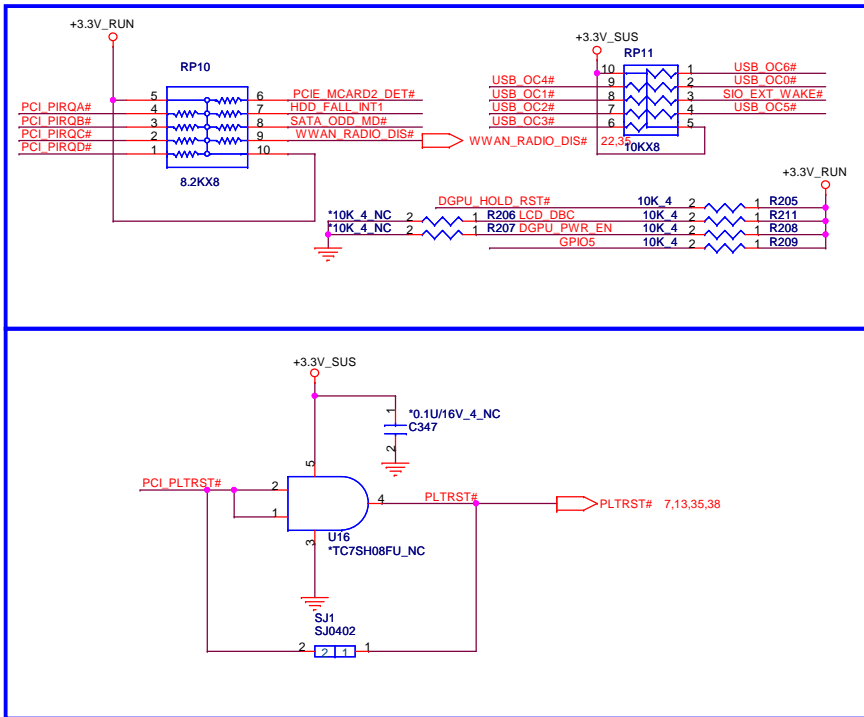


Take care while using GPIO19 for Hot Plug function

PCH Strap Table

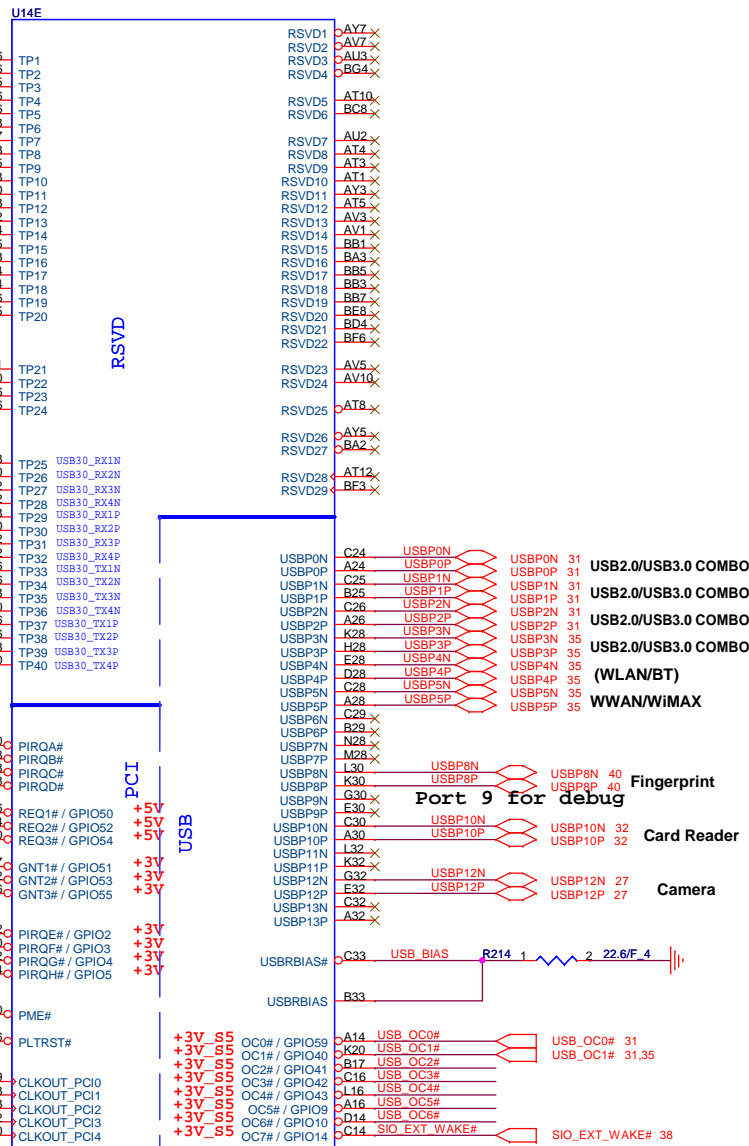
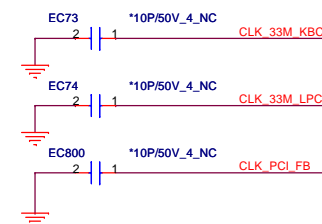
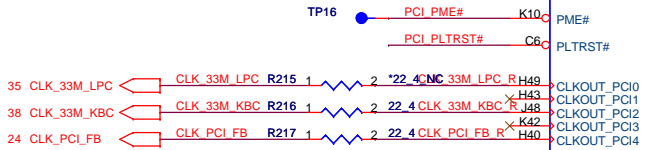
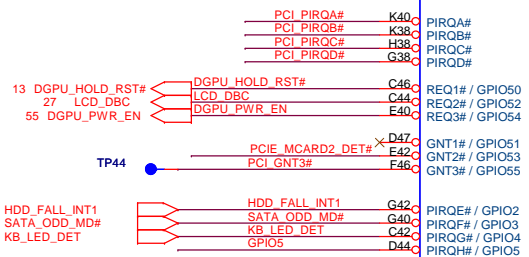
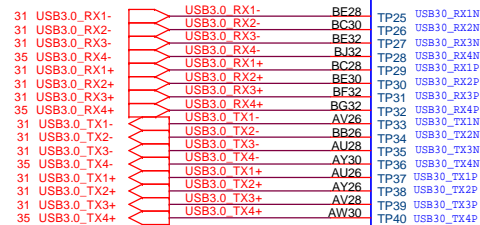
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○R203 1 2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○R204 1 2 1K 4 ACZ_SYNC_R

Cougar Point-M/Panther Point (PCI,USB,NVRAM)



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESl strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><td>Bit 0</td><td>Bit 1</td><td>Boot Location</td></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]												
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									

USB3.0

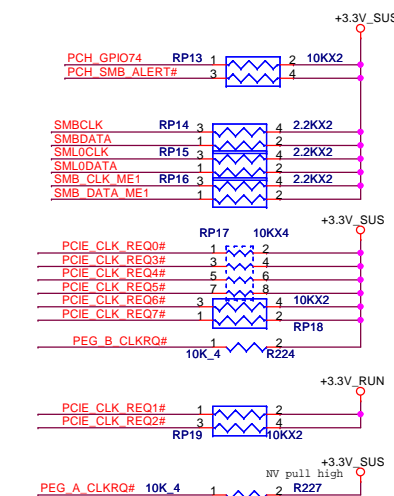
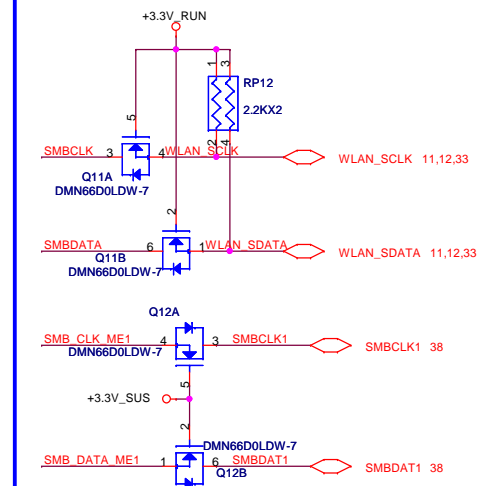


U14B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



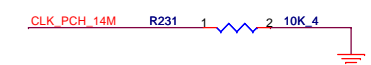
	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode

**Quanta Computer Inc.**

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Panther Point 5/7

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Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO

BMBUSY#

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

HOST ALERT#1

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

MFG-TEST

WLAN_RADIO_DIS#

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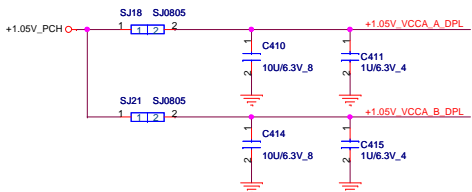
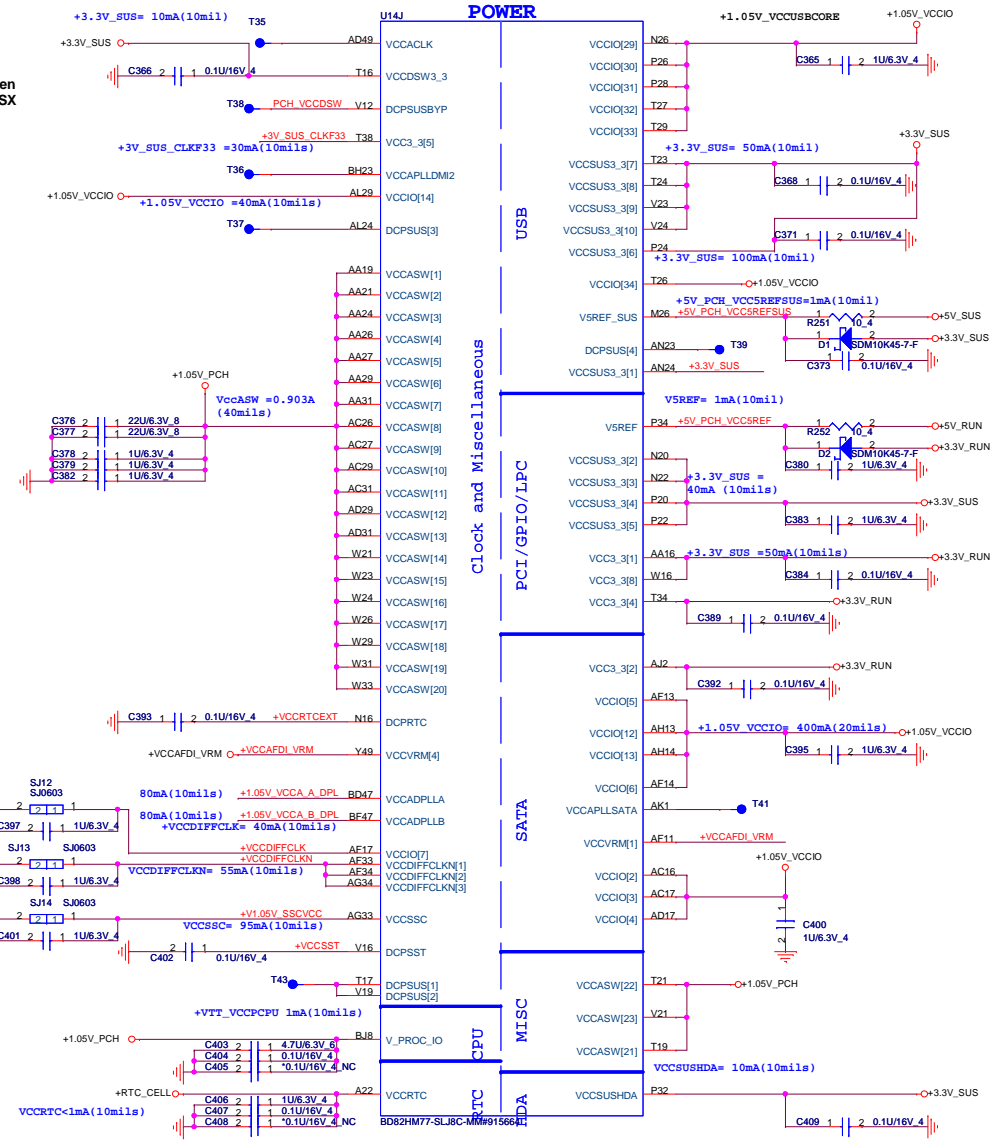
Size Document Number

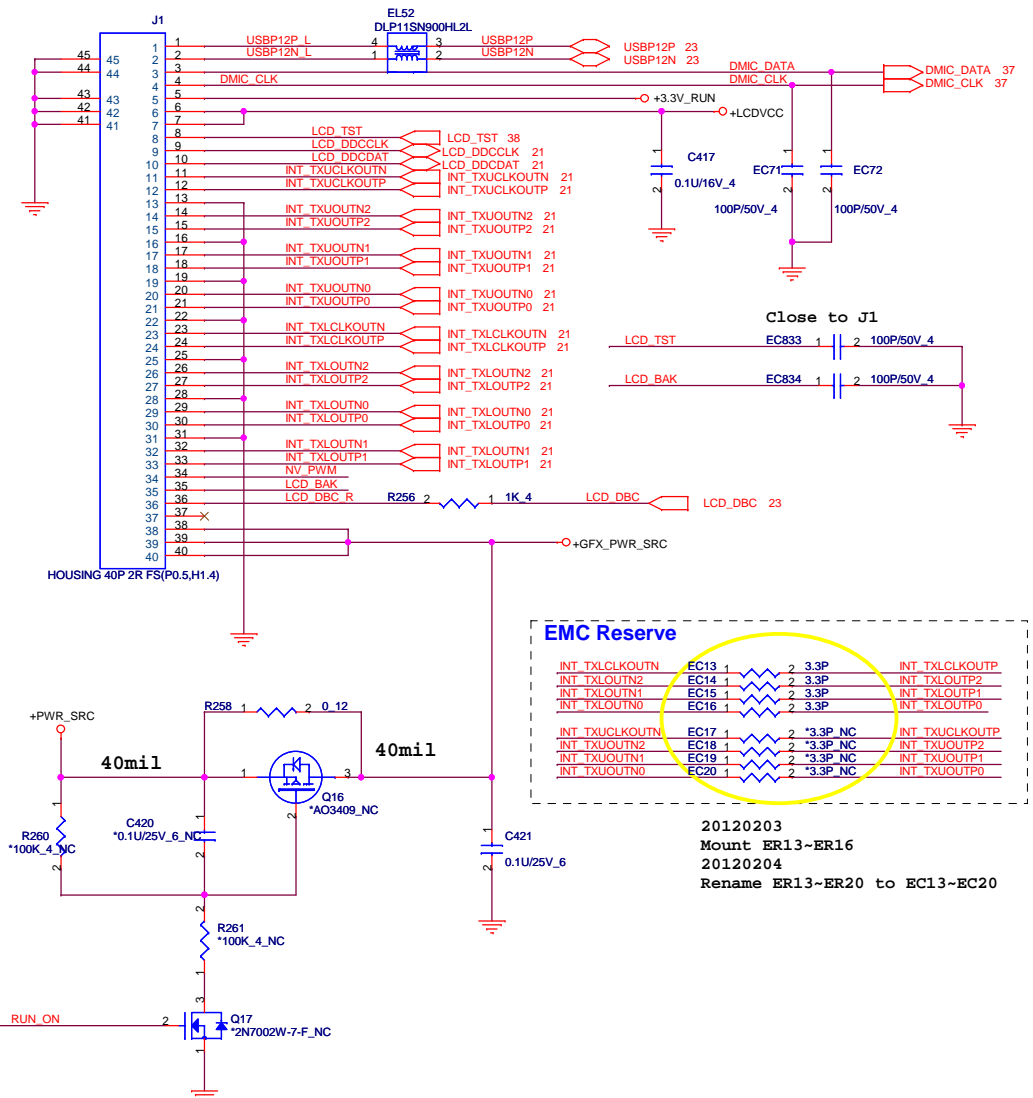
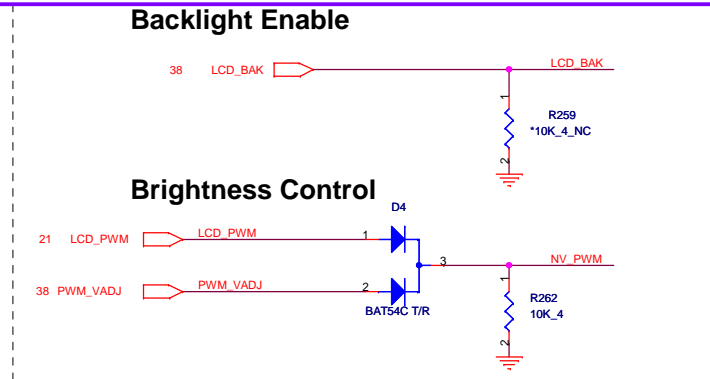
Panther Point 6/7

Date: Monday, February 13, 2012 Sheet 25 of 55

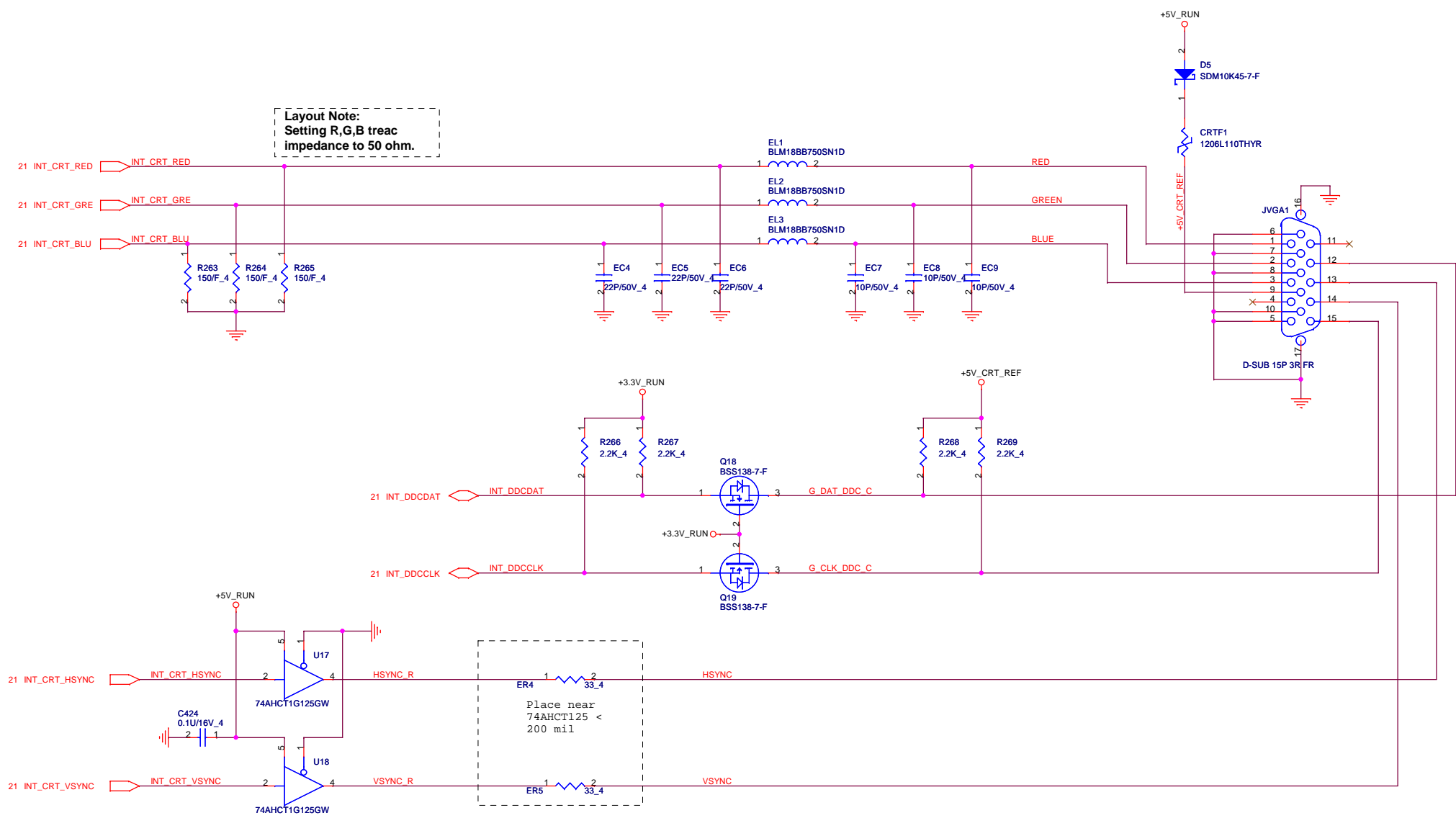
Rev 1A

Cougar Point/Panther Point (POWER)





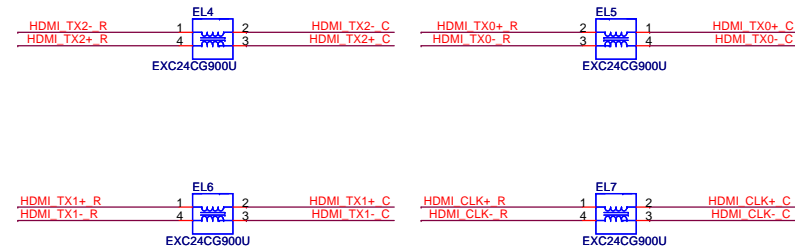
Layout Note:
Setting R,G,B treac
impedance to 50 ohm.



HDMI

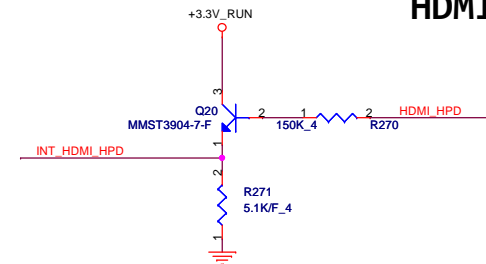
21 INT_HDMI_TXP2	INT_HDMI_TXP2	C425	1	2	0.1U/16V_4	HDMI TX2+ R
21 INT_HDMI_TXN2	INT_HDMI_TXN2	C426	1	2	0.1U/16V_4	HDMI TX2- R
21 INT_HDMI_TXP1	INT_HDMI_TXP1	C427	1	2	0.1U/16V_4	HDMI TX1+ R
21 INT_HDMI_TXN1	INT_HDMI_TXN1	C428	1	2	0.1U/16V_4	HDMI TX1- R
21 INT_HDMI_TXP0	INT_HDMI_TXP0	C429	1	2	0.1U/16V_4	HDMI TX0+ R
21 INT_HDMI_TXN0	INT_HDMI_TXN0	C430	1	2	0.1U/16V_4	HDMI TX0- R
21 INT_HDMI_TXCP	INT_HDMI_TXCP	C431	1	2	0.1U/16V_4	HDMI CLK+ R
21 INT_HDMI_TXCN	INT_HDMI_TXCN	C432	1	2	0.1U/16V_4	HDMI CLK- R
21 HDMI_SCL	HDMI_SCL					
21 HDMI_SDA	HDMI_SDA					
21 INT_HDMI_HPD	INT_HDMI_HPD					

Reserve for EMI and close to HDMI CONN



HDMI_HPD spec VinH_min=2.0V

HDMI HPD

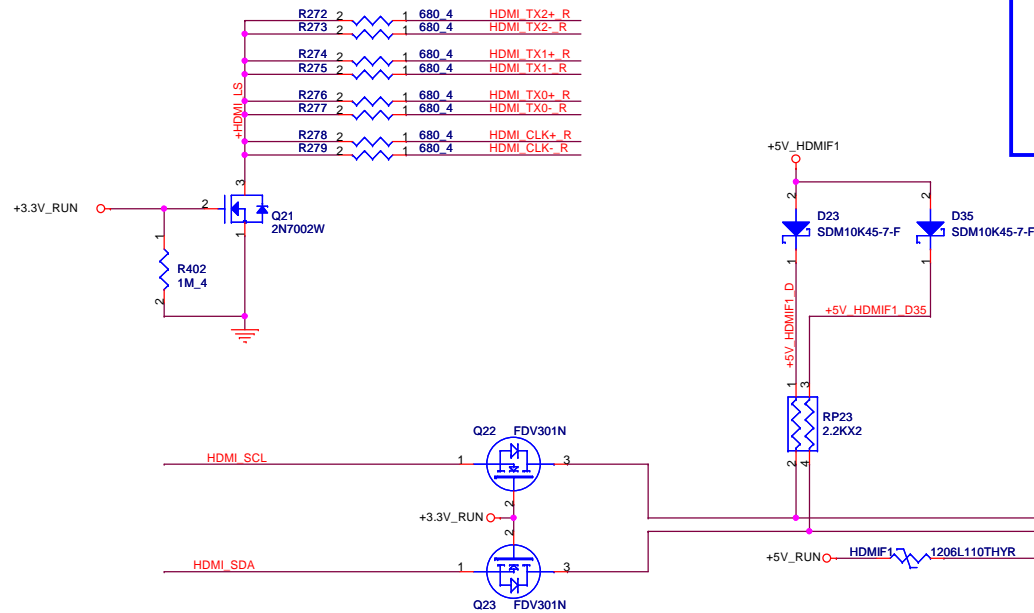


$$IB = (5V - 0.7V) / (150K + (70 + 1) 5.1K) = 8.4\mu A$$

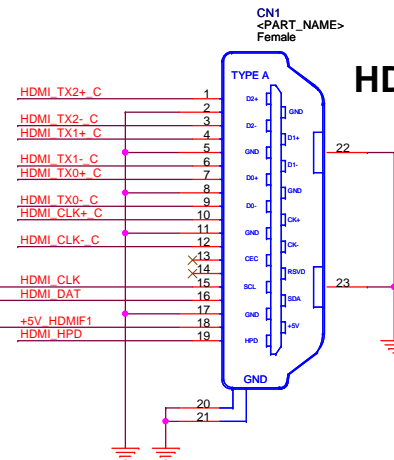
$$IE = (1 + 70) \times 8.4\mu A = 596.4\mu A$$

$$VE = 596.4\mu A \times 5.1K = 3.04V$$

$$B = 70$$



HDMI Conn.



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	A	B	C	D	E
4					
3					
2					
1					



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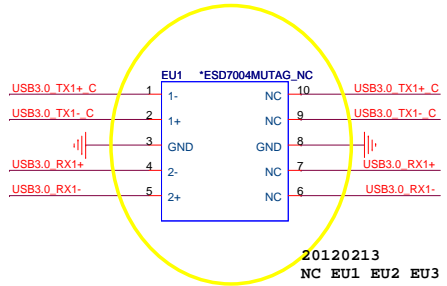
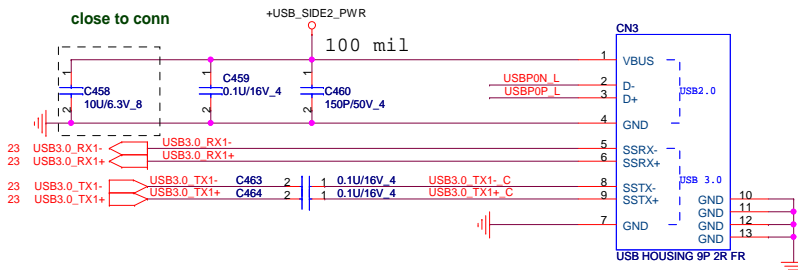
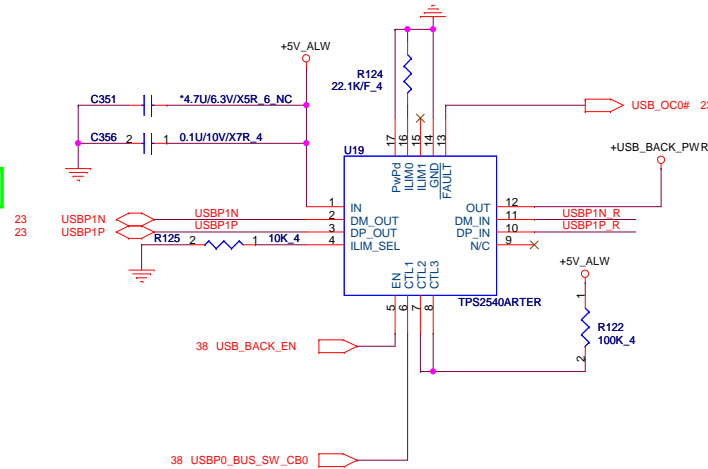
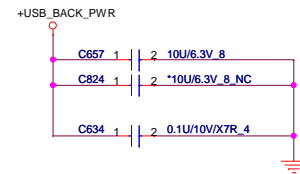
Size	Document Number	Rev
	NA	1A
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USB Power share

USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

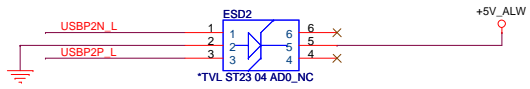
	R109	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Applied Now

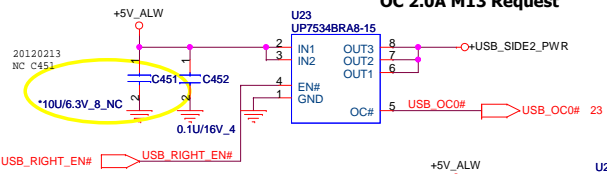


ESD Function

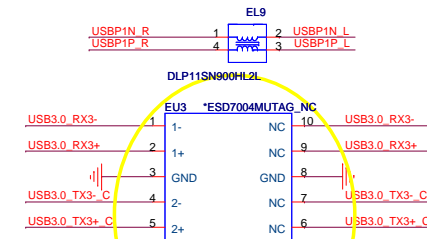
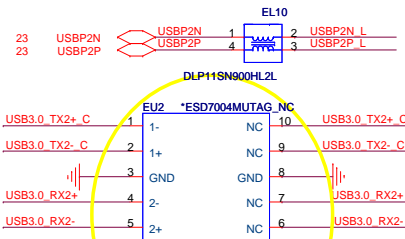
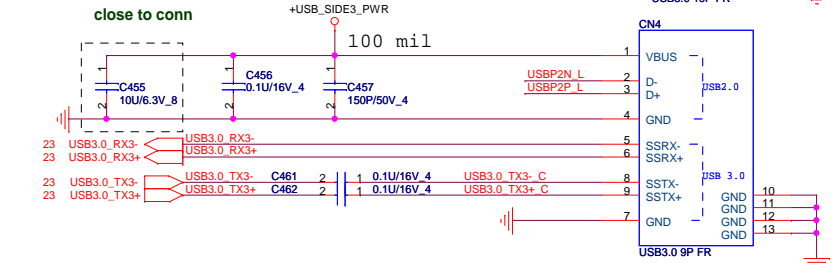
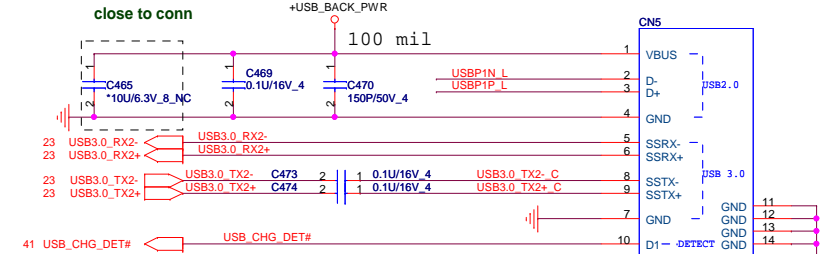
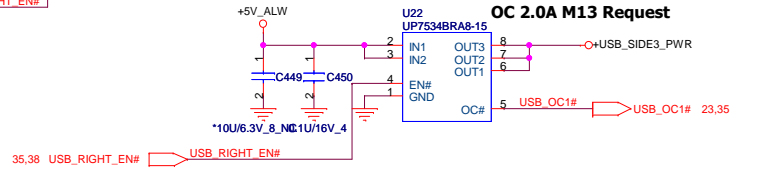
Place ESD diodes as close as USB connector.



I continuous 1.5A OC 2.0A M13 Request



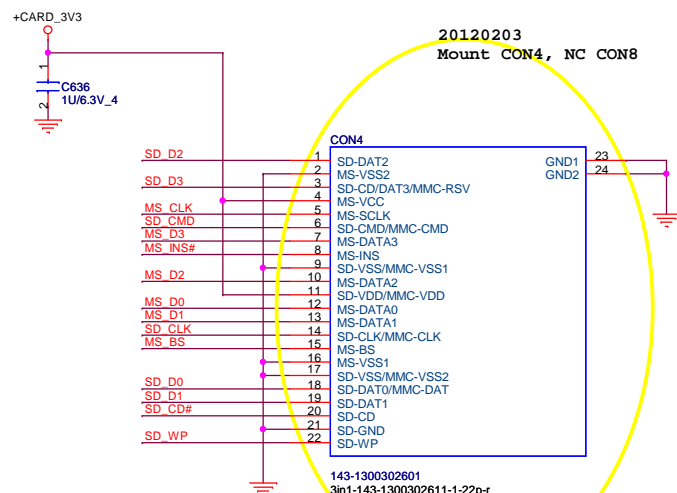
I continuous 1.5A OC 2.0A M13 Request



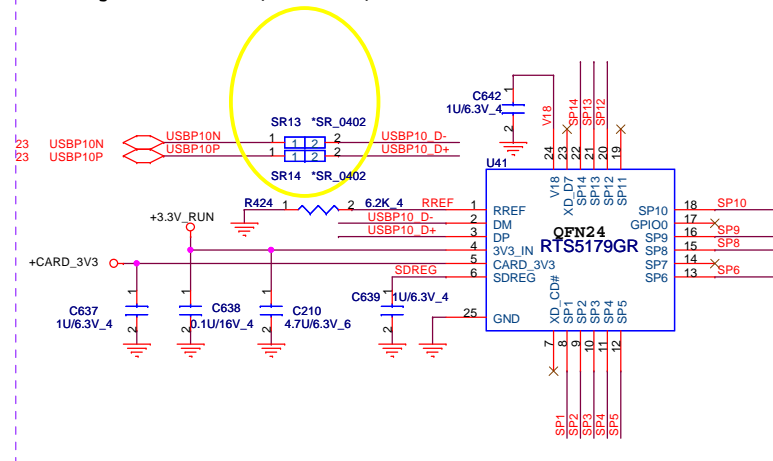
ESD Function

Cardreader (RTS5179GR) Support SD3.0 USH50

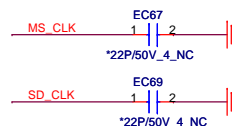
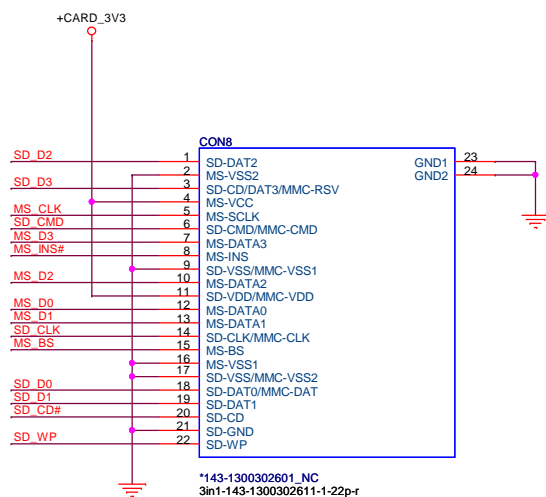
For Vostro Placement(V08,V08A)-Far ODD



20120206
Remove EL47
Change R210 to SR13(short0402)
Change R212 to SR14(short0402)



For INSPIRON Placement (R08,R08A,R08T)-Near ODD



SP1	SD_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

Share Pin



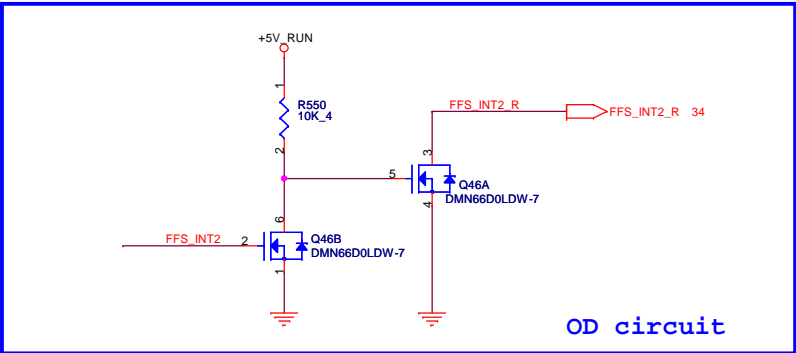
Quanta Computer Inc.

PROJECT : R08

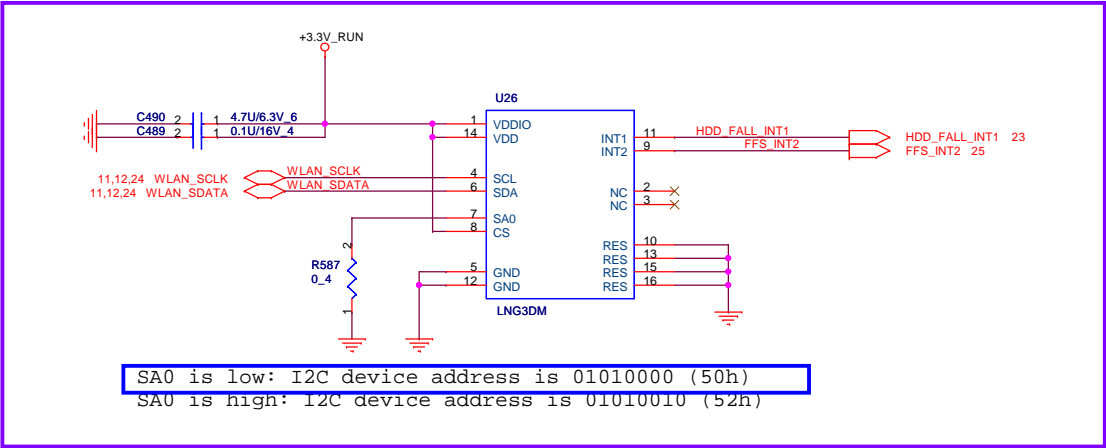
Size	Document Number	Rev
	Cardreader (RTS5179GR)	1A
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3-axis Fall Sensor

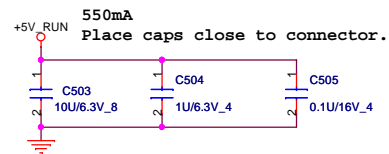
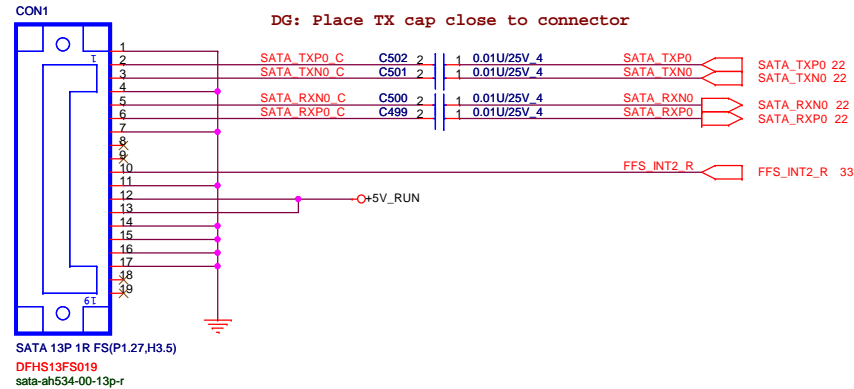
If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit



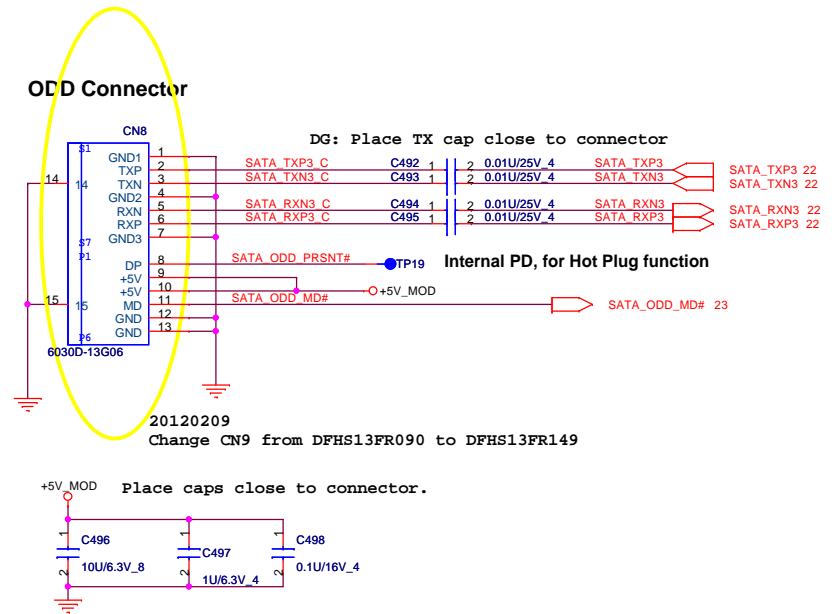
20120203
Mount Function code "FFS" part



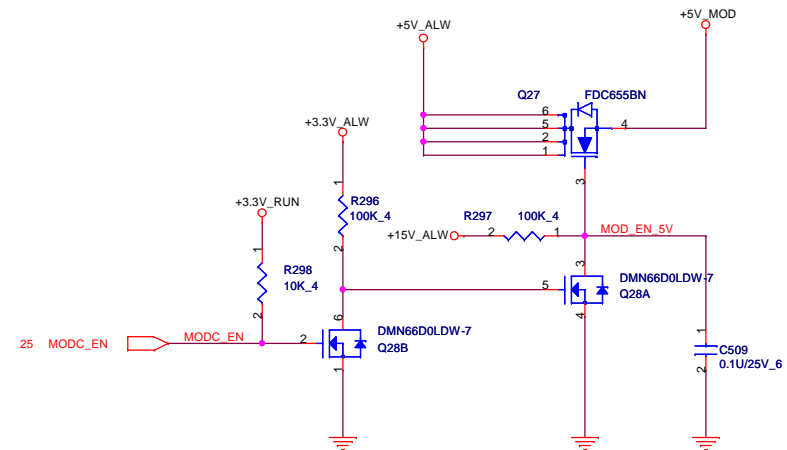
HDD



ODD



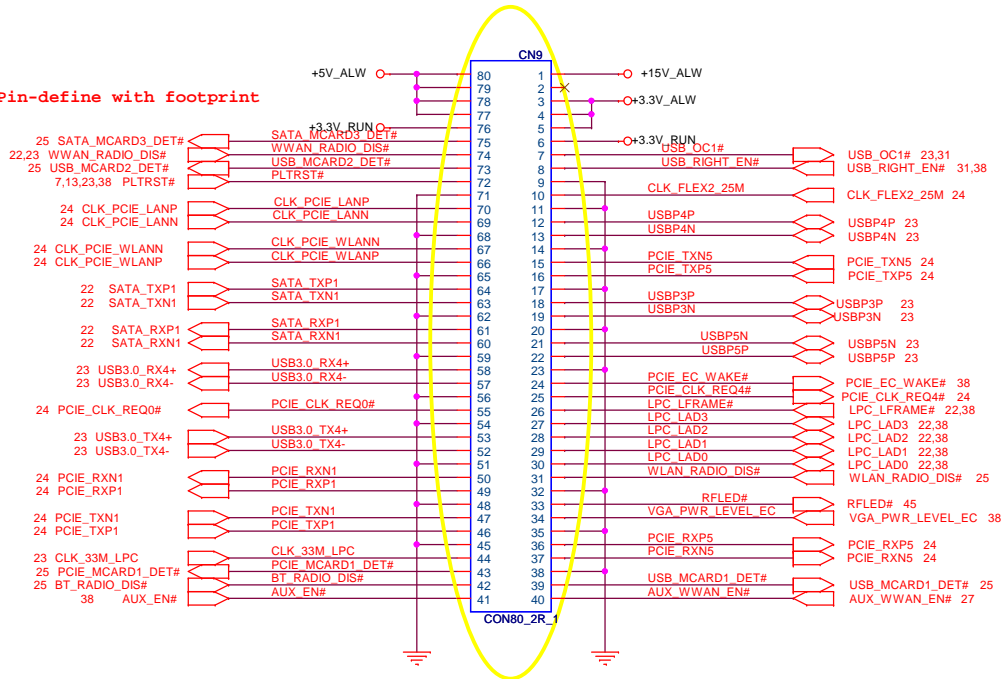
Support Zero power ODD



20120203

Change CN9 footprint from "88069-8001b-bs-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"

Check Pin-define with footprint

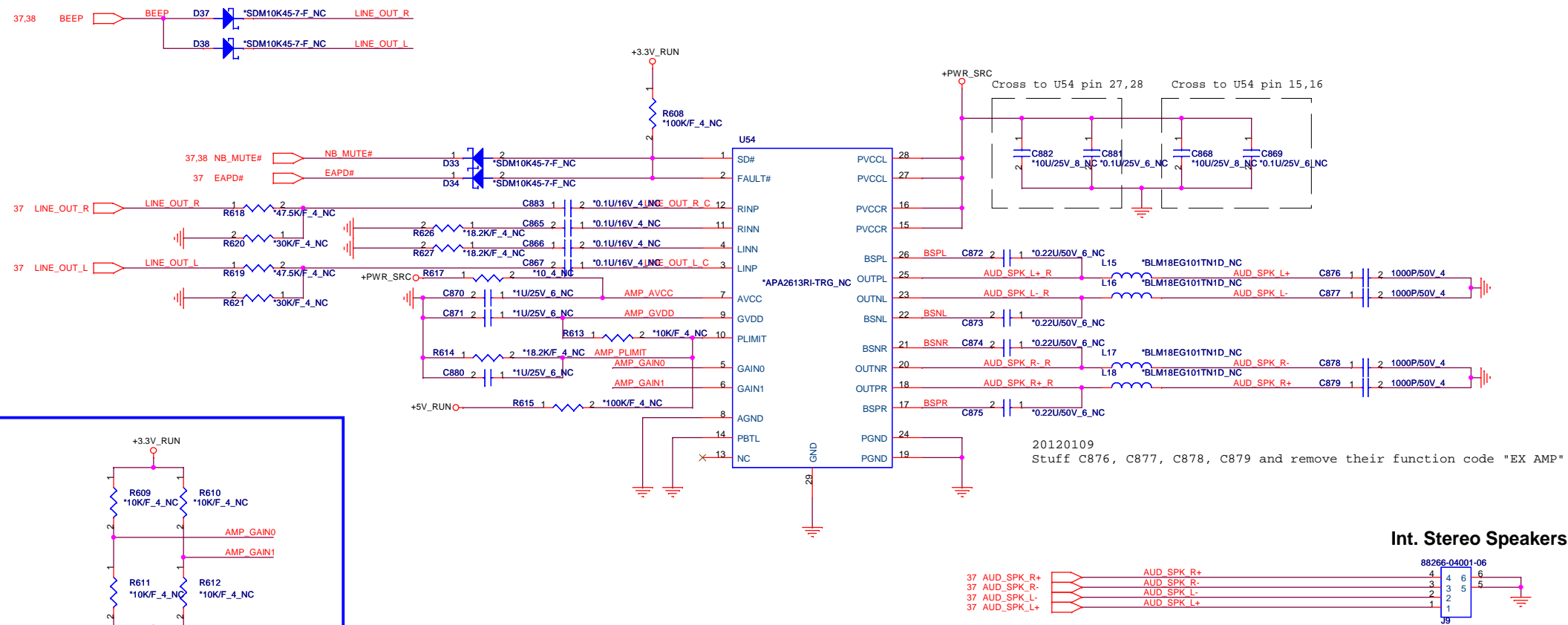


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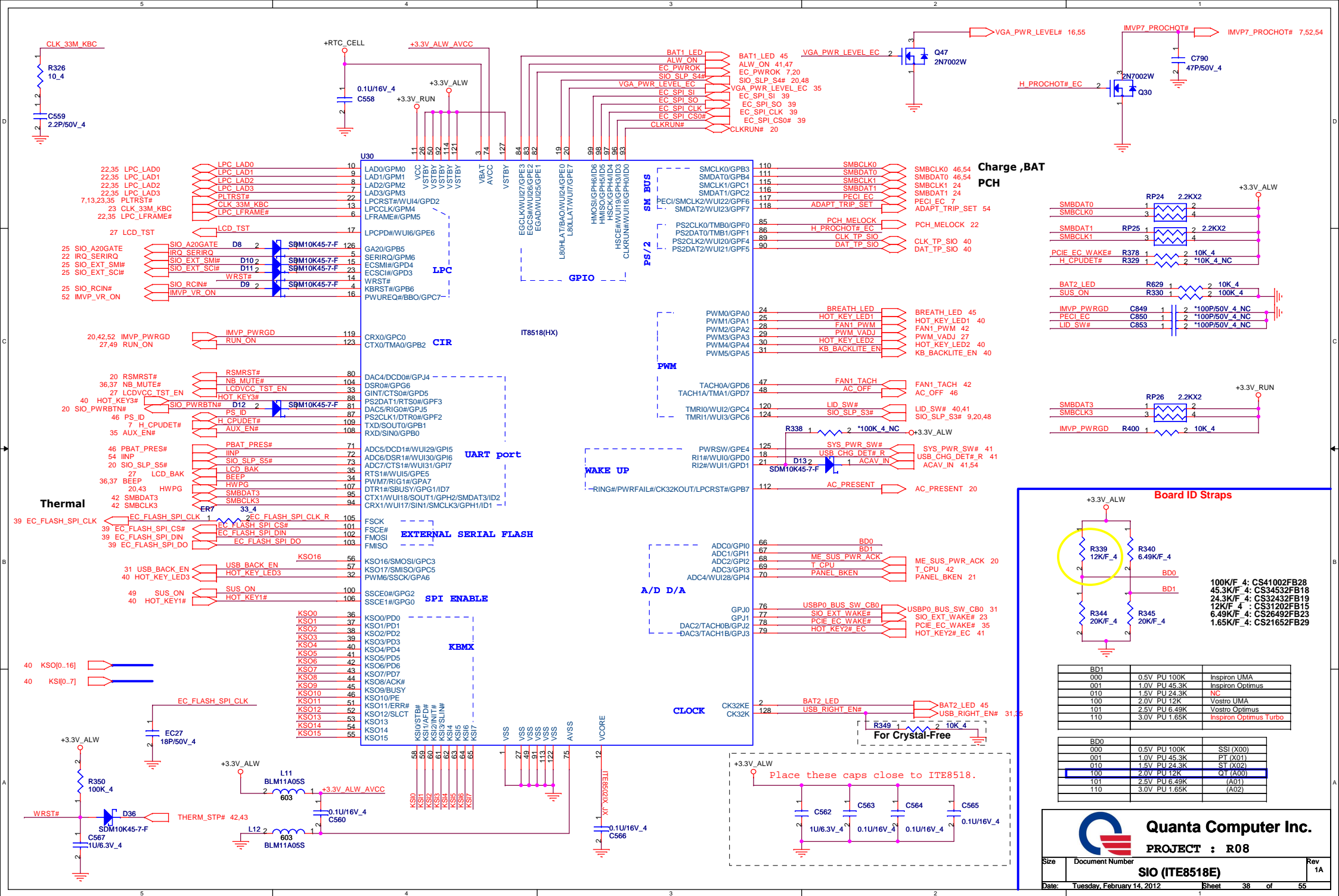
Size	Document Number	Rev
	BTB CONN	3A
Date:	Monday, February 13, 2012	Sheet 35 of 55

ANPEC APA2613 is P2P to TI TPA3113 Default use APA2613



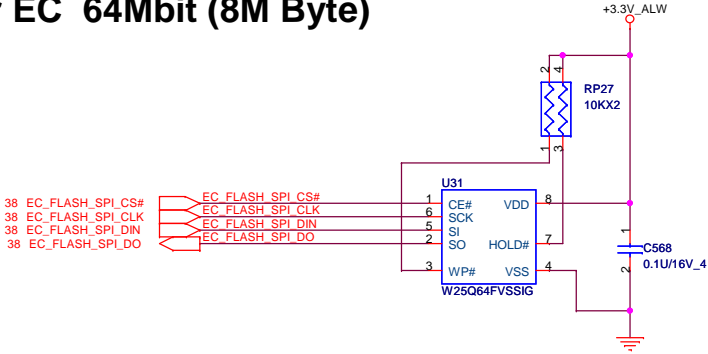
GAIN1	GAIN0	AMPLIFIER GAIN (dB)
		TYP
0	0	20
0	1	26
1	0	32
1	1	36

	Amplifier	Function code
R08/R08A/V08/V08A	CODEC CX20672	Mount "IN AMP"
R08T	APA2613 or TPA3113	Mount "EX AMP"

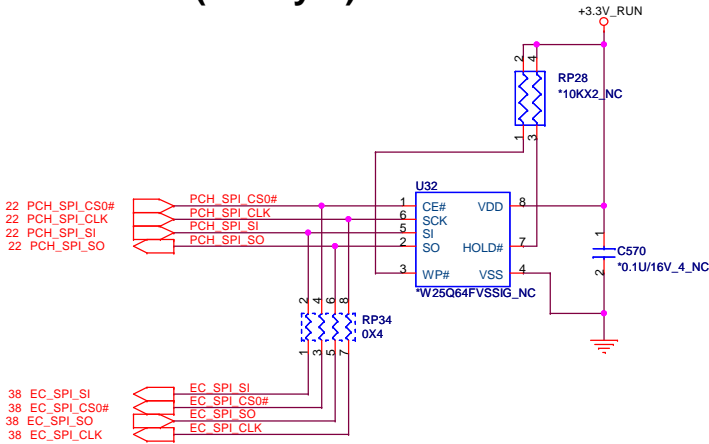


FLASH / RTC

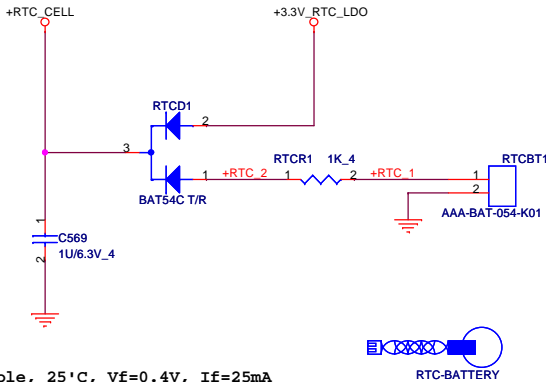
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)



RTC



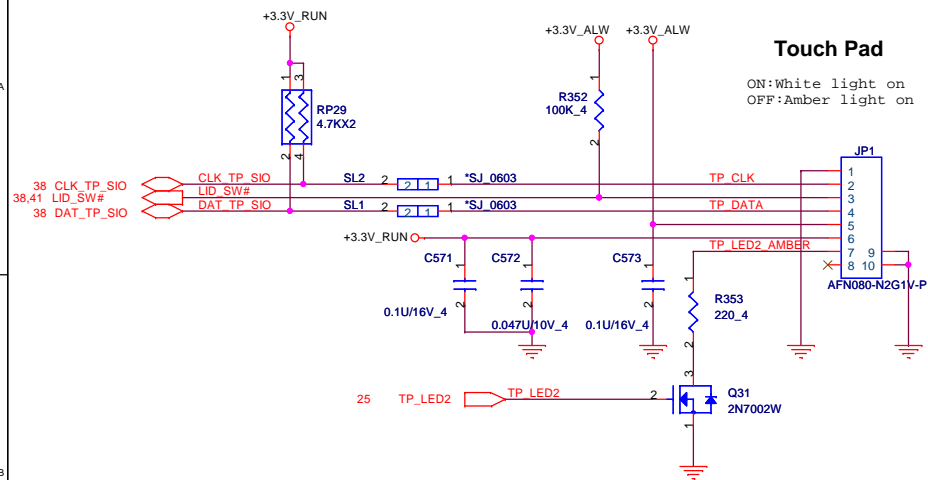
Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA



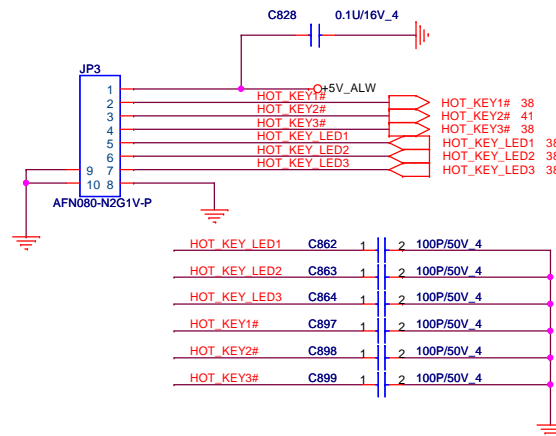
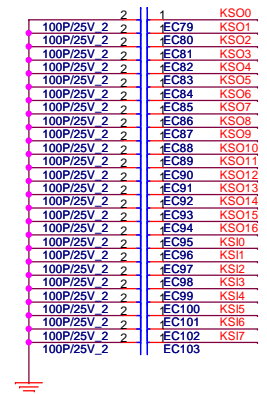
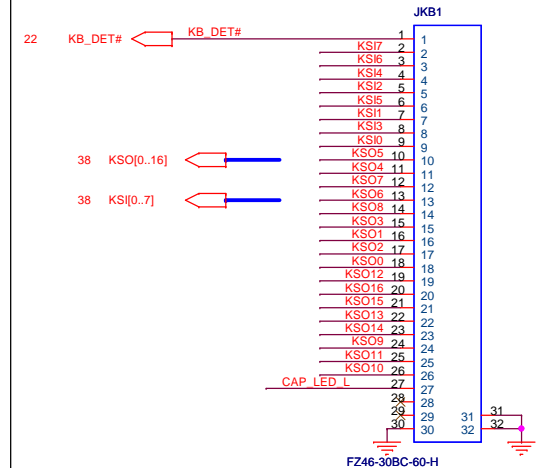
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TP CONNECTOR

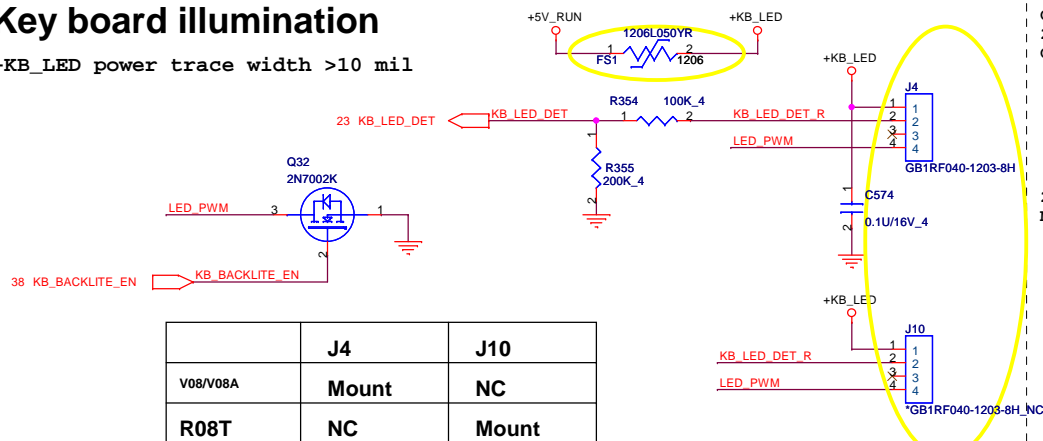


HotKey CONN

**KB CONN**

Key board illumination

```
+KB_LED power trace width >10 mil
```



20120206

Change FS1 to SR12(short1206)

20120213

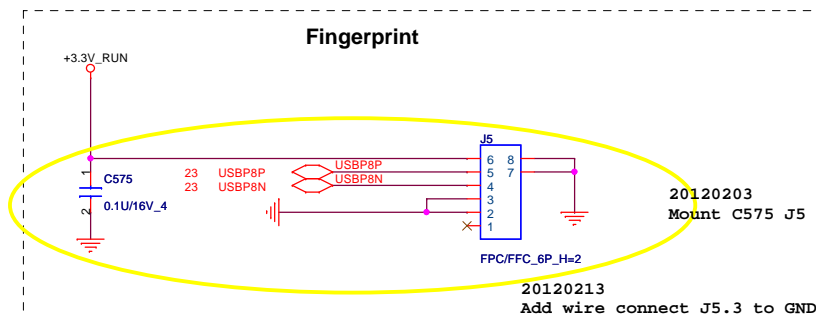
Change SR12 back to FS1

20120203

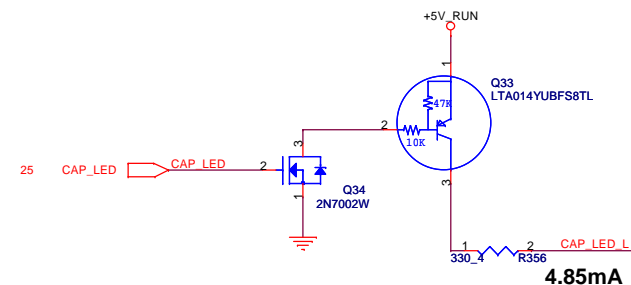
Mount J4, NC J10

	J4	J10
V08/V08A	Mount	NC
R08T	NC	Mount

Fingerprint



20120213
Add wire connect J5.3 to GND


$$V_{i(on_max)} = -1.4V$$
$$V_i(\text{off_min}) = -0.3$$


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TP / KB

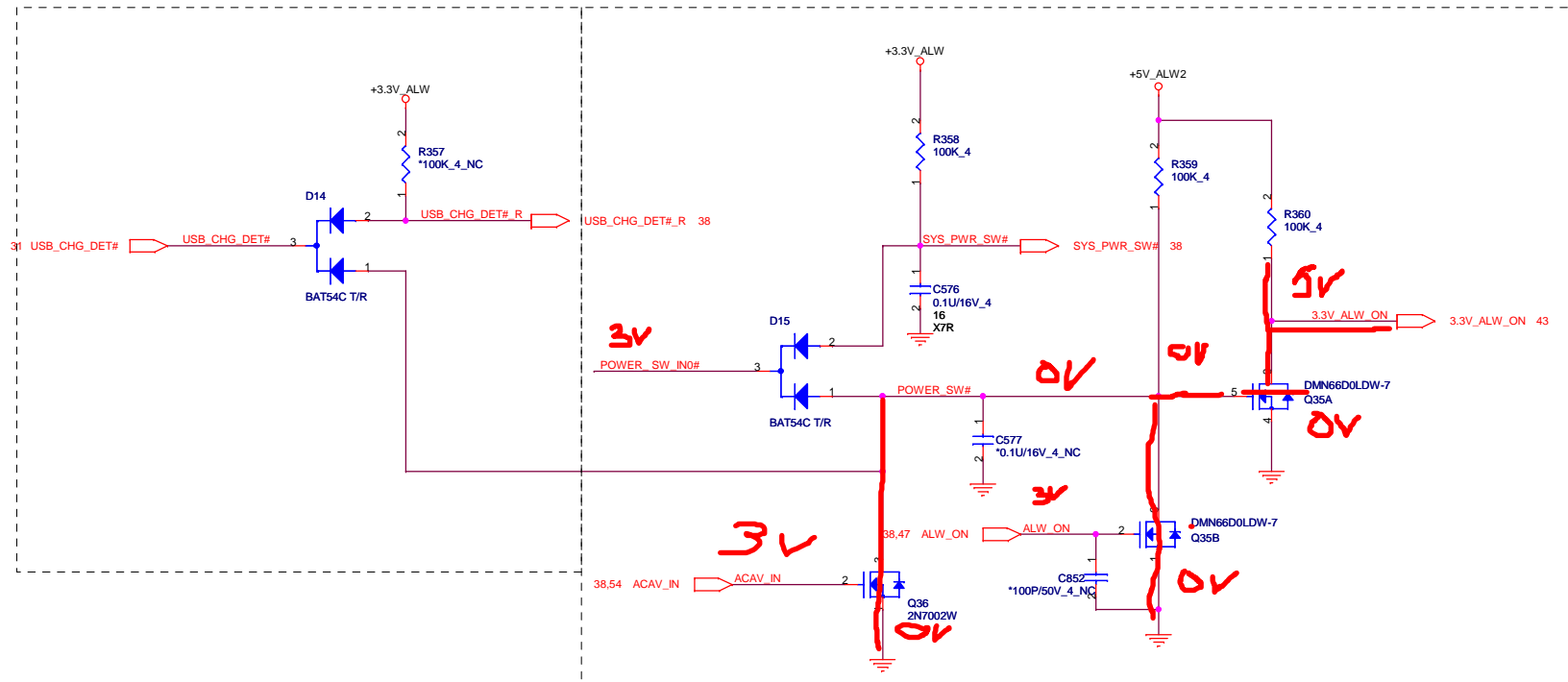
Date: Monday, February 13, 2012

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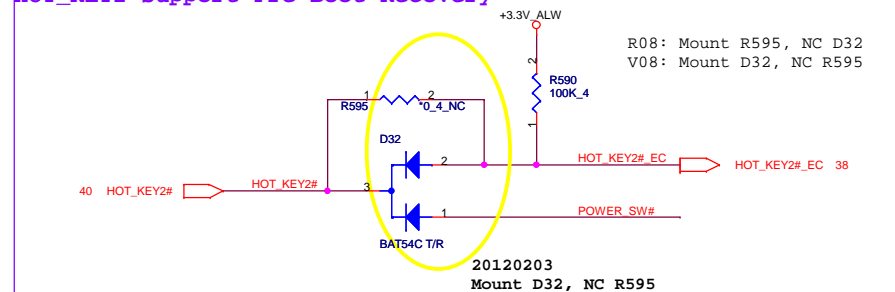
rev

For USB charger usage

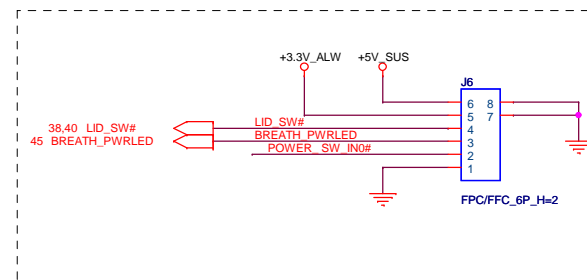
3V ALW ON POWER LOGIC

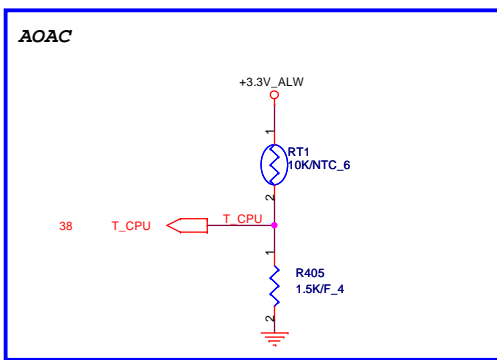


HOT_KEY2 support Pre-Boot Recovery

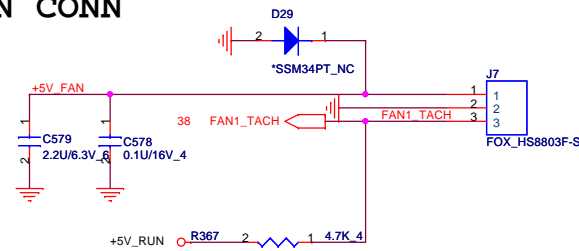


TO PWR button board



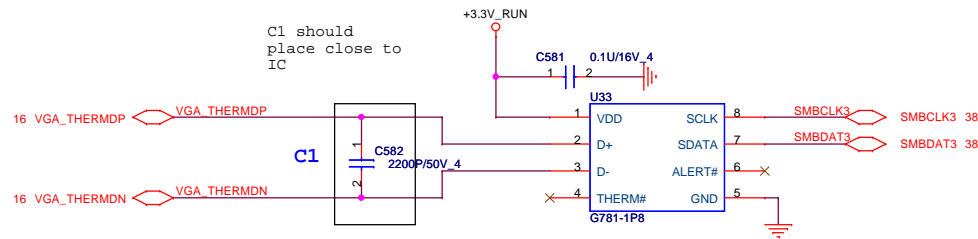


FAN CONN



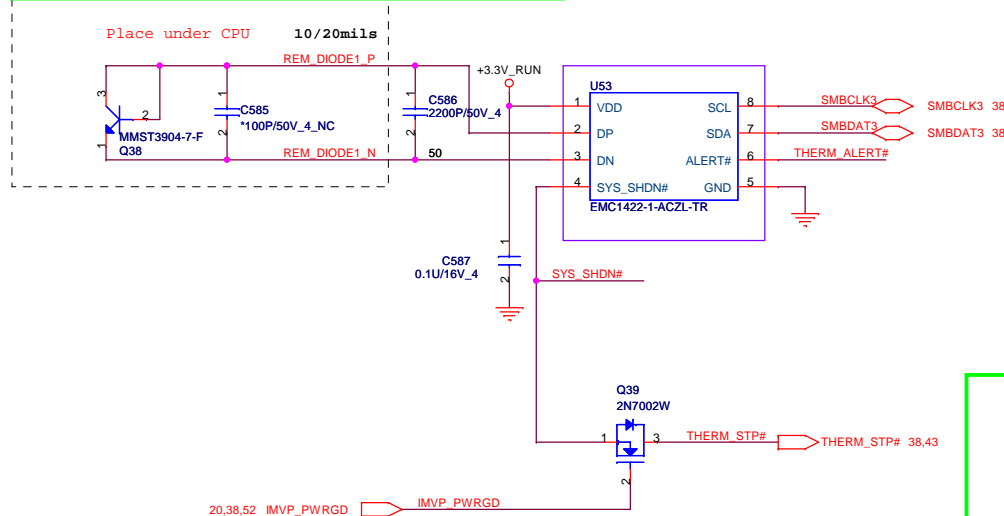
G781-1P8

SMBus address is 1001101xb (9Ah) (x is R/W bit).



THERMAL IC

1. Place C586 close to EMC1422-U1
 2. Place C585 to be close to Q38
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C586, then C585 should be dummy

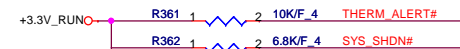


EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	4.7K	77°C	83°C	89°C	95°C	101°C
6.8K	78°C	84°C	90°C	96°C	102°C	108°C
10K	79°C	85°C	91°C	97°C	103°C	109°C
15K	80°C	86°C	92°C	98°C	104°C	110°C
22K	81°C	87°C	93°C	99°C	105°C	111°C
33K	82°C	88°C	94°C	100°C	106°C	112°C

CHECK OTP WITH Thermal.

OTP 85 degree C



EMC1422

OTP 85 degree : R361 = 10K, R362 = 6.8K
OTP 90 degree : R361 = 6.8K, R362 = 10K

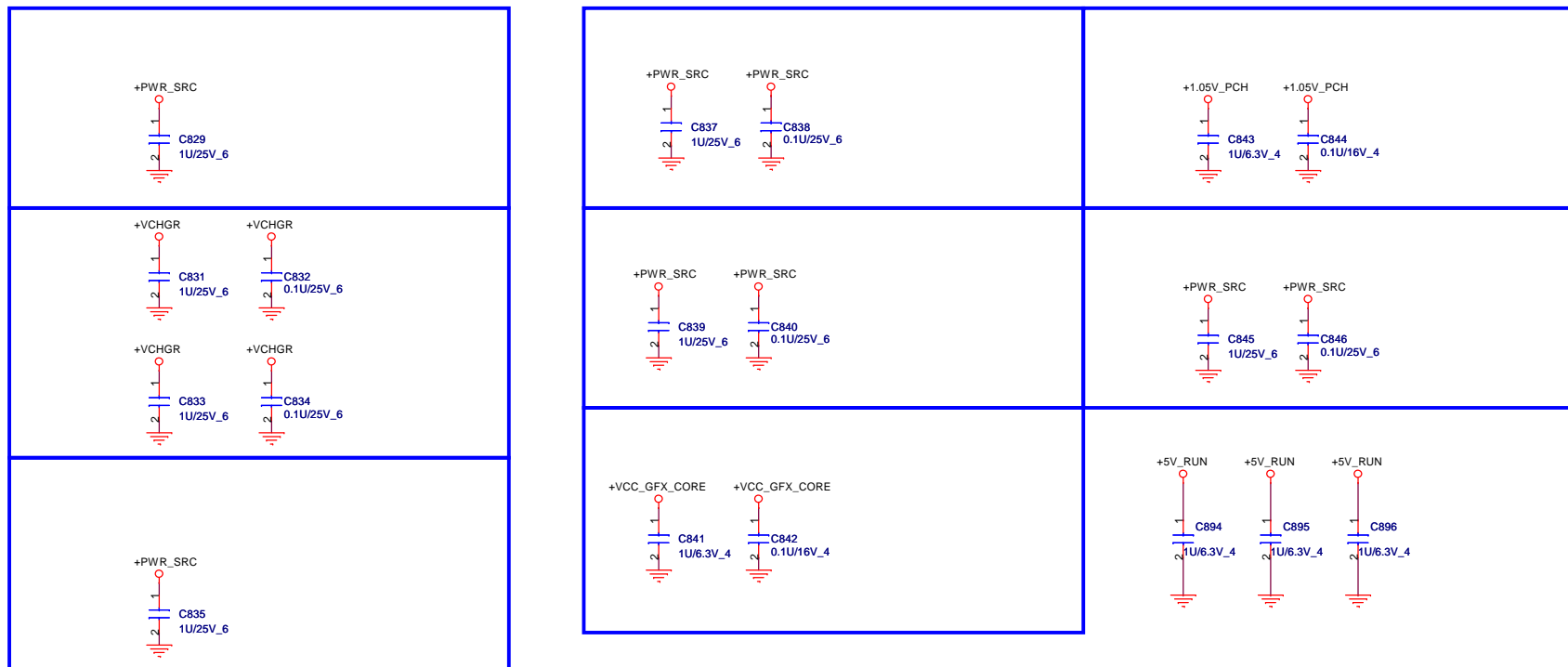
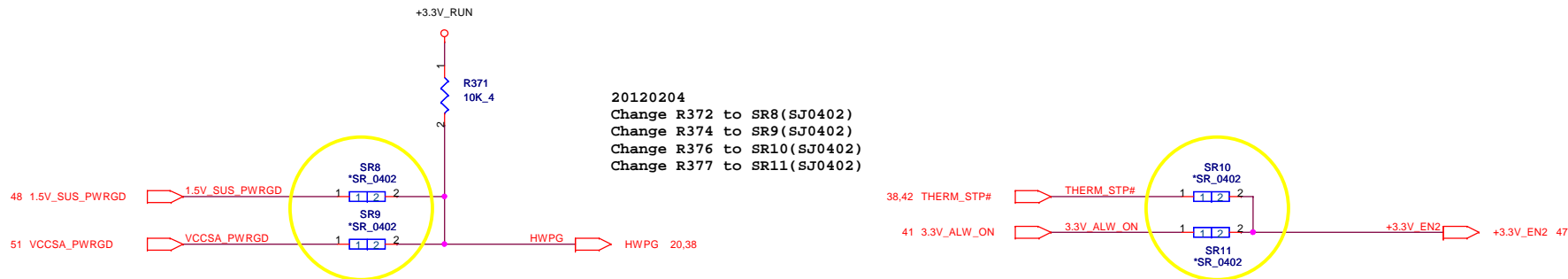
NTC7718W

OTP 85 degree : R361 = 18.7K, R362 = 2K
OTP 91 degree : R361 = 10.5K, R362 = 7.5K



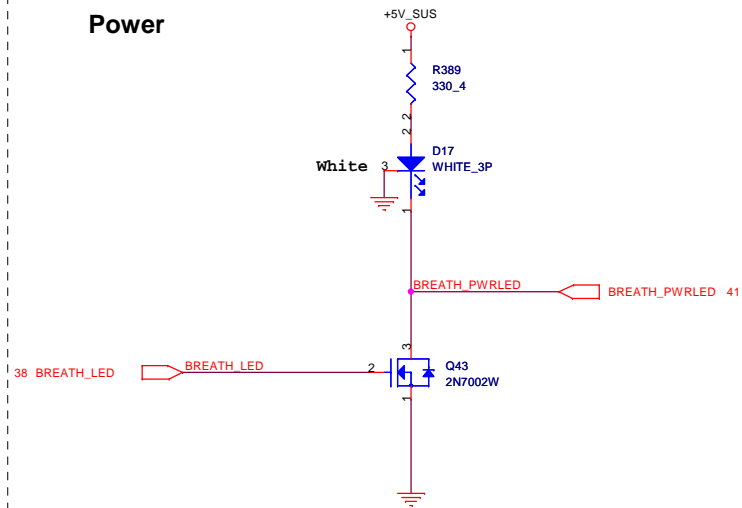
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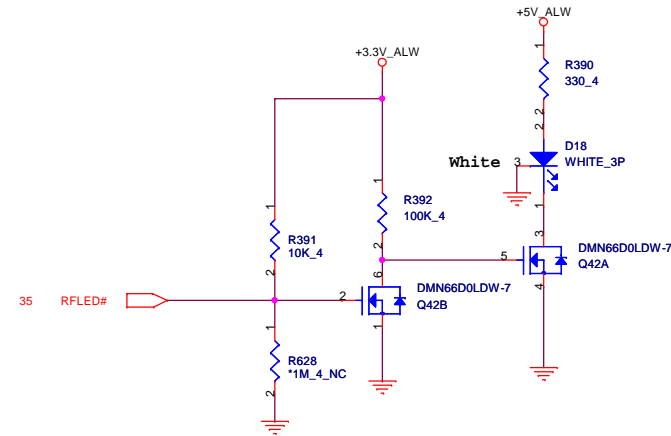




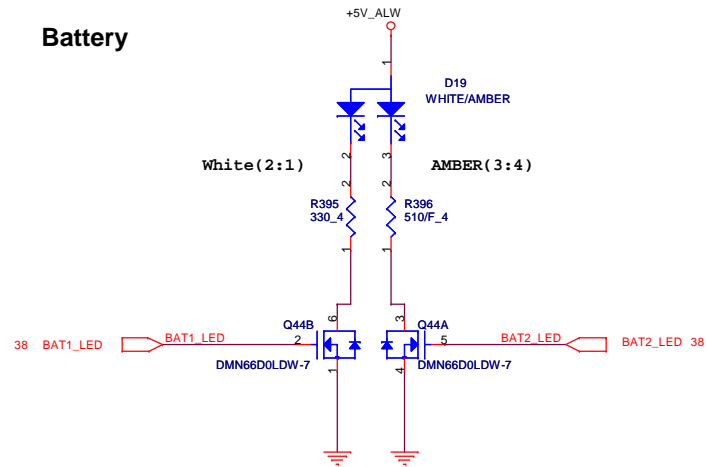
Power



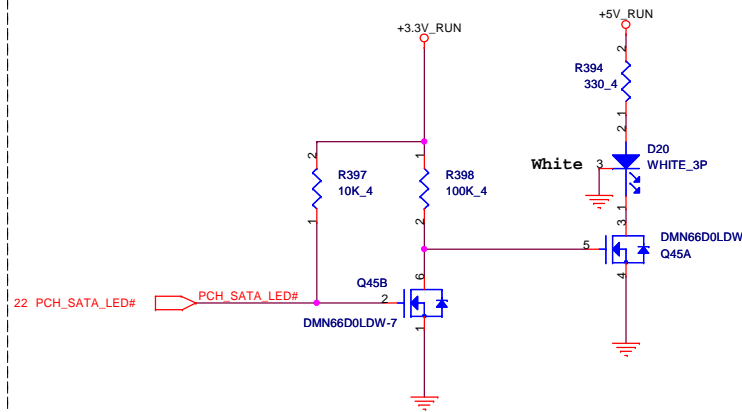
Bluetooth / WLAN on/off LED



Battery



HDD activity LED.



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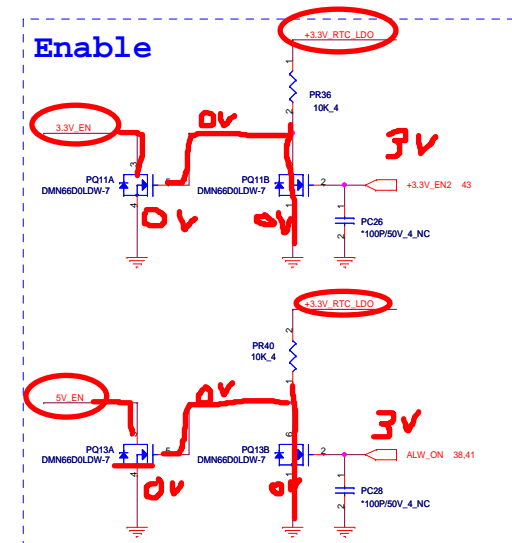
Size Document Number Rev
1A

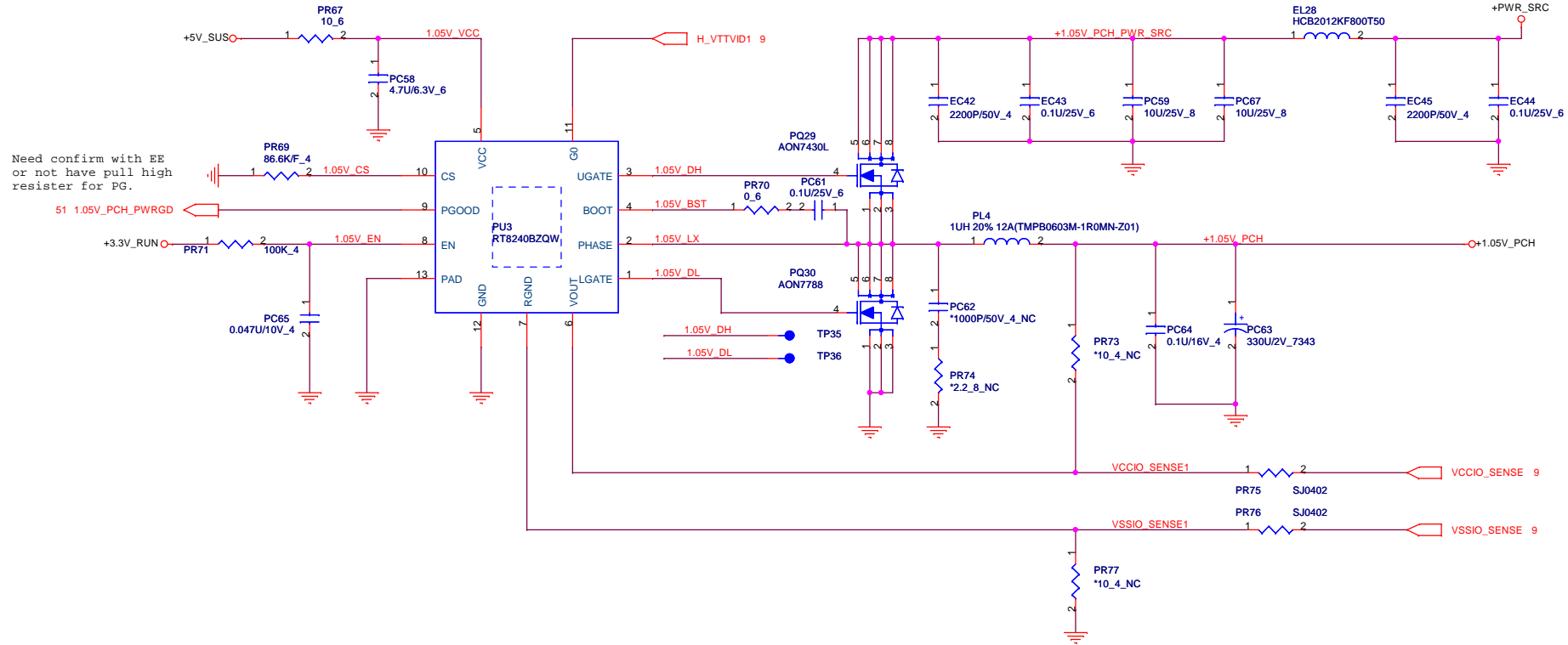
LED

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TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz





+1.05V_PCH
1.05 Volt DC +/- 2%
Fsw : 400K
TDC : 13.5A
OCP : 19.5A



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	+1.05V_PCH / VTT (RT8240BGQW)	1A
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CPU Power

